Firmware lower-level discrimination and compression applied to streaming x-ray photon correlation spectroscopy area-detector data

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We present a data acquisition system to perform on-the-fly background subtraction and lower-level discrimination compression of streaming x-ray photon correlation spectroscopy (XPCS) data from a fast charge-coupled device (CCD) area detector. The system is built using a commercial frame grabber with a built-in field-programmable gate array (FPGA). The system is capable of continuously processing 60 CCD frames per second each consisting of 1,024 × 1,024 pixels with up to xx photon hits per frame.

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I. INTRODUCTION

X-ray photon correlation spectroscopy (XPCS) performed with hard x-rays ($E \gtrsim 7$ keV, where E is the x-ray energy) has emerged as a powerful technique for characterizing the equilibrium or steady-state dynamics of condensed matter on length scales shorter than can be achieved with optical techniques and on longer time scales than can be achieved via neutron scattering. Even on optically accessible length scales, opaque and metallic samples are readily studied, providing new opportunities for studies of colloidal and other soft matter systems. Several recent review articles[1–3] provide summaries of the scientific impact of the technique and the mechanics of performing such experiments.

A key factor enabling XPCS's recent significance has been the application of direct-detection area detectors to problems of interest—so-called multispeckle XPCS—because even at a third generation synchrotron source like the Advanced Photon Source (APS), XPCS experiments are brilliance limited. Area detectors allow x-ray speckle data to be simultaneously collected at equivalent wave-vector transfers (Q's) permitting averaging of the auto-correlation functions thereby improving the signal-to-noise ratio (SNR) in an experiment. Simultaneously, area detectors collect data over a span of different wave-vectors greatly increasing the efficiency of such experiments. Despite recent successes, however, the use of such detectors remains challenging both because of the limited availability of suitable high-speed detectors and because of the need to gather, manage and reduce data at increasingly higher frame rates over increasingly long measurement durations. This paper addresses the second issue, namely development of a system to compress x-ray-speckle data on-the-fly so that XPCS-suitable detectors can be run as fast as possible for as long as possible in an operationally-sensible manner.

As a specific example, we consider recent multi-speckle XPCS measurements that were performed at our beamline (8-ID) at the Advanced Photon Source (APS). Over a very narrow temperature range, a dense colloidal suspension in a binary mixture was found to display novel repulsive- and attractive-glass behavior with an unusual transition between these two phases[4]. The complex phase behavior was unraveled via a combination of small-angle x-ray scattering (SAXS) and XPCS measurements. The dynamics (XPCS) measurements required collecting instantaneous speckle patterns at 60 frames per second (fps) over collection periods extending to 1,000 seconds. Intensity-intensity time correlations, calculated according to

$$g_2(Q, \Delta t) = \frac{\langle I(Q,t) I(Q, t+\Delta t)\rangle_t}{\langle I(Q,t)\rangle_t^2},$$

where Δt is the delay time and $I(Q,t)$ is the intensity at wave-vector Q and time t, revealed a distinct 2-step decay of the correlation functions in the repulsive-glass phase followed by a fully arrested correlation function in the attractive-glass phase. In between these 2 phases, the time autocorrelation functions exhibited a very unusual logarithmic intensity decay. The unusual dynamic properties of this system, spanning nearly 5 decades in delay time, could not have been discovered and measured without an area detector running continuously at high frame rates over extended collection periods.

Despite the evident scientific need, the measurements described above are not operationally-sustainable without the developments described below. The detector used for the above measurements[5] has 1,024 × 1,024 14-μm-square pixels and outputs 2 bytes of data per pixel. Without compression, a single time sequence as described above would require more than 120 gigabytes (GB) of storage. Since, in the example above, 100's of time sequences were required to establish and confirm the phase diagram of the system, disk space and data-reduction

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bandwidth would be rapidly exhausted. A key realization is that i) we use direct-detection CCD's for XPCS so the signal above the background (dark noise) is relatively high meaning individual photons can be distinguished and ii) the scattered signal is weak so the number of recorded photons per frame is relatively small. Thus, each frame can be compressed by a significant amount—typically xx%.

During the first iteration of software development for the camera[5], the frames were accumulated in computer memory and then compressed and written to disk when the memory was full. This allowed the camera to run at full speed (60 fps) but only accumulate ≈ 1,000 frames or 3 decades in delay times. A second iteration of high-level software (C++) development performed compression and wrote the data to disk on-the-fly. But even with a relatively powerful workstation computer dedicated to this task, on-the-fly compression performed with this software was unable to process 60 fps so the short-time dynamic range of the detector was limited. As such, we were led to consider firmware thresholding and compression of rapidly streaming multi-speckle XPCS data.

The remainder of this paper describes the design, implementation and performance of this system. We used a field-programmable gate array (FPGA) hosted on a commercial frame grabber to realize live lower-level discrimination (LLD) and compression of multi-speckle XPCS data. The output of the system is a series of highly-compressed data frames each consisting of a listing of intensities above a user-determined threshold and their locations on the CCD sensor. Somewhat analogous work has been described recently[6] but though the frame rate was significantly higher than for our detector, the mean number of events per frame was much smaller. Reference 7 discusses direct-detection CCD's, dark noise and photon identification in the context of multi-speckle XPCS measurements.

II. SYSTEM DESIGN

A schematic overview of our multi-speckle real-time compression system is shown in Fig. 1. It consists of a fast area detector[5], a signal translator (not shown) that converts the low-voltage differential signaling (LVDS) signal of the detector to Camera Link, a frame grabber and a host workstation with fast local storage. Aside from the detector, the frame grabber is the key component in the system. It is a Dalsa Anaconda PCI-X frame grabber with an on-board Xilinx Virtex-Pro XC2VP20 FPGA. Solid arrows indicate data flow. The arrow heads indicate the direction of data flow and the width of the arrow is proportional to the data rate. Dashed arrows indicate the control interface for the system which has been developed under the EPICS areaDetector[8] framework.

The key step in the system that reduces the data flow is compression which is accomplished via implementation of an appropriate LLD[5] in the FPGA. Briefly, as each

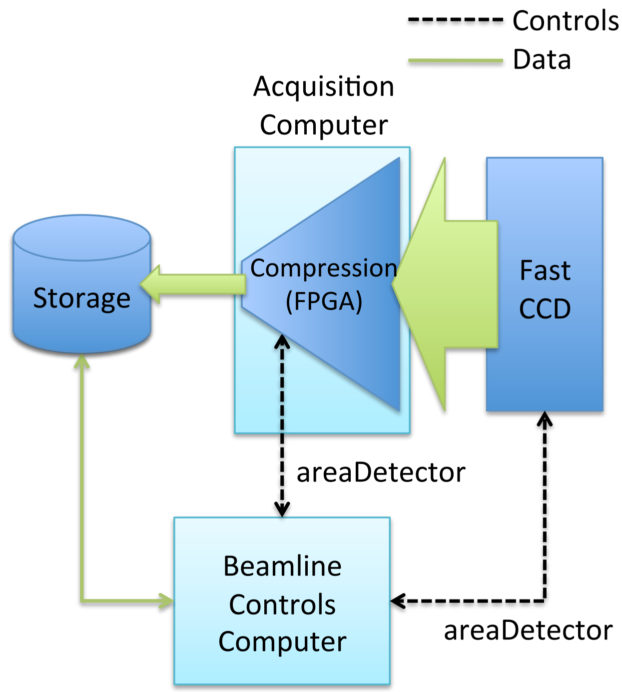

FIG. 1. Schematic representation of the data flow from detector to disk.

frame is streamed through the FPGA, pixels are retained if they equal or exceed a defined LLD value and discarded otherwise. The LLD is specified on a pixel-by-pixel basis according to the following equation:

$$\mathrm{THRESHOLD}(i,j) = \mathrm{C} + \mathrm{DK}_{\mathrm{AVE}}(i,j) + \alpha \mathrm{DK}_{\mathrm{RMS}}(i,j), \quad (1)$$

where (i,j) are pixel indices, C is a pixel-independent constant threshold or offset value, $\mathrm{DK}_{\mathrm{AVE}}$ is the pixel-dependent value of the average dark signal, and $\mathrm{DK}_{\mathrm{RMS}}$ is the pixel-dependent value of the root-mean-square (rms) of the dark signal multiplied by a scaling factor β. In practice, the average dark value is first subtracted from all incoming data frames and then the dark-subtracted frames are compared to the LLD defined in Eqn. 1 with $\mathrm{DK}_{\mathrm{AVE}}(i,j) = 0$.

The LLD array can be created and updated on-the-fly in the FPGA on an as-needed basis. Figure 2 illustrates the procedure and the subsequent data compression. If only a constant LLD is required, then a LLD value specified by the user on a control screen is loaded into the FPGA. If, as is more typically the case, the LLD includes dark subtraction and a linear combination of a constant and the rms dark frame then the procedure is as follows.

1. The user specifies how many dark frames, $N_{\mathrm{DARK}}^{\mathrm{AVG}}$, should be collected to determine the average dark signal. $N_{\mathrm{DARK}}^{\mathrm{AVG}}$ dark frames are accumulated and recursively averaged and then stored on disk.

2. The user specifies how many dark frames, $N_{\mathrm{DARK}}^{\mathrm{RMS}}$,

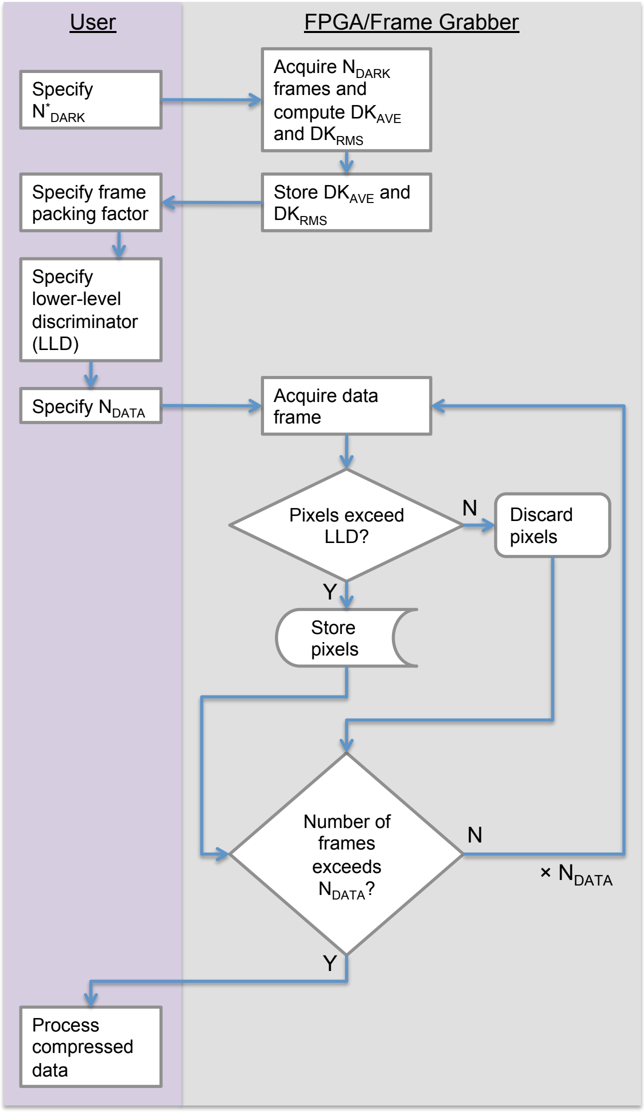

FIG. 2. Schematic of dark and data acquisition processing steps. For simplicity, the flow chart shows the number of dark frames being the same for the average and rms determination, but this need not be the case.

should be collected to determine the rms dark signal. (In practice, we use $N^{\mathrm{RMS}}_{\mathrm{DARK}} = N^{\mathrm{AVG}}_{\mathrm{DARK}} \equiv N_{\mathrm{DARK}}$.) $N^{\mathrm{RMS}}_{\mathrm{DARK}}$ dark frames are accumulated and, using the mean dark frame determined in Step 1, the mean absolute deviation (MAD) is recursively determined and stored on disk. (The MAD is more easily calculated in the FPGA than the variance.) Provided that the variance in the dark signal is well approximated by a normal distribution, which we will show below to be the case for the detectors we use, then the standard deviation or rms is given by $\sqrt{(\pi/2)}\mathrm{MAD}$.

3. The user specifies the frame packing ratio. Within a continuous sequence of data acquisition, the

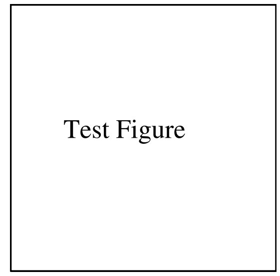

FIG. 3. Dark image and dark mean and variance.

frame grabber requires a fixed frame size so the FPGA can not output variably-sized compressed data frames to the frame grabber. Moreover, it is inconvenient to constantly change the frame buffer size in the image grabber as signal levels change. Instead, the FPGA packs the user-specified integer number, N_{pack}, of compressed frames into a single uncompressed frame and then passes the packed frames to the frame grabber. This procedure reduces the rate of data flow from the frame grabber to the computer bus by $N_{\mathrm{pack}}\times$. Typical packing ratios used in our experiments are 4 or 8 or 16.

4. The user specifies the LLD according to Eqn. 1.

Steps 1–4 need only be repeated occasionally Thereafter, the number of frames, N_{DATA} to accumulate in a sequence is specified and the detector accumulates compressed frames and writes them to local or network-attached storage.

Details about how and/or in what format the frames are compressed to in software before writing to disk.

Describe FPGA architecture and development.

Describe how FPGA is controlled via higher level software.

Itemize data acquisition modes.

III. SYSTEM PERFORMANCE

Describe performance of the system.

Itemize properties of dark—mean and variance—and how variance is approximated in the FPGA.

Itemize properties of incoming data and processed data

Results (and graphs) of compression factors and max frame rates versus compression factors.

IV. CONCLUSIONS

We have successfully implemented an FPGA-based system for on-the-fly thresholding and compression of rapidly streaming multi-speckle XPCS data. The system allows us to acquire and compress 1 megapixel CCD frames at $\geq$ 60 fps allowing XPCS to measure delay

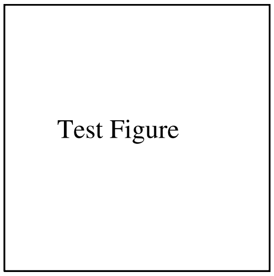

FIG. 4. Raw image and different thresholding.

times spanning at least 5 orders of magnitude. Future work will focus on extending the current 32-bit architecture to 64-bit architecture and physically-separating the FPGA unit from the frame grabber. The former will allow us to support newly emerging faster XPCS-suitable detectors[9] and the latter will provide more flexibility with respect to choice of frame grabbers while, at the same time, allowing a stable FPGA development environment. We are also considering implementing so-called "droplet" algorithms[7] or performing multi-tau correlations directly in the FPGA[10]. A drawback of the latter though is that it would restrict its application to only stationary systems despite the significant progress that has been realized lately with respect to non-equilibrium and intermittent dynamics[11–13]. In this regard, a more promising future development is to marry the pre-processing described in this paper, with correlations performed via high-performance computing (HPC). The inherently parallel nature of multi-speckle XPCS suggest that firmware thresholding combined with HPC can yield autocorrelation functions in real time.

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