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OPTICAL DETECTOR TEAM

Next Generation detector Controller (NGC). Support Document

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(ENGDC). ODT discussions

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The purpose of this document is to compile in a single source some of the idiosyncrasies of FIERA and IRACE in order to ease any discussion about the optimum architecture of a possible next generation detector controller at ESO. This document is limited to the technical aspects of the hardware and sets aside software issues.

1 Introduction

Both FIERA and IRACE have been developed in parallel and close connection. From an electrical point of view they do basically the same and only differ in few internal details which have been oriented to perform better with one type of detector that with another. Both FIERA and IRACE can indistinguishably bias a piece of semiconductor, be it a CCD or an infrared detector. Both controllers can toggle the detector clock lines with a programmable and seamlessly timing, and with an adjustable clock voltage swing. Both controllers can sample at an arbitrary position in time the output video signal from the detector; and both controllers can digitize the video signal with 16-bit ADCs and put the image in the workstation memory. See Figure 1-1. Therefore, there are no reasons to believe that one of the two controllers is a functional superset of the other or, that one of the two, with some small modifications, is not able to read an image from a detector it has not been designed for.

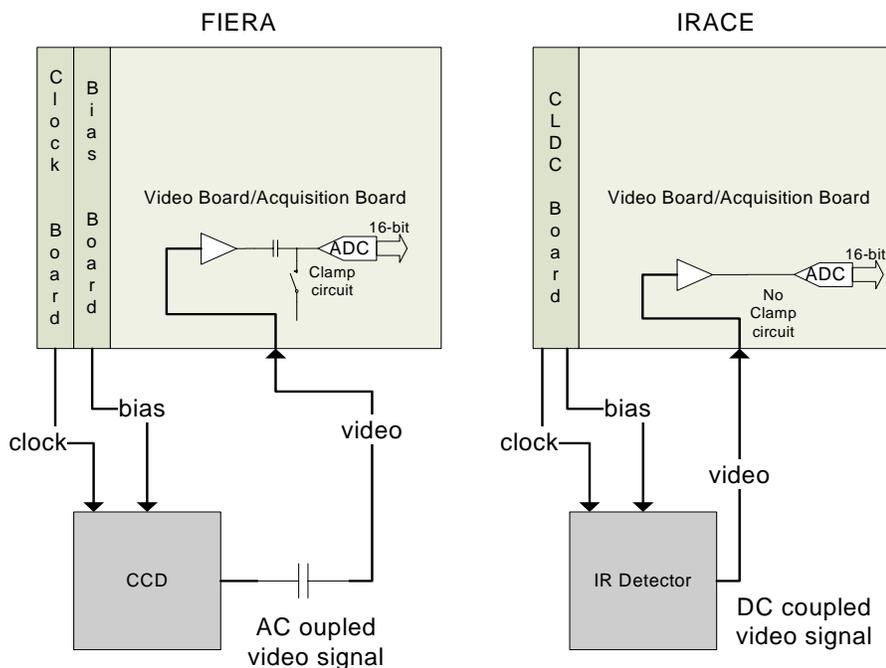


Figure 1-1 Overview of FIERA and IRACE

2 FIERA and IRACE. electrical characteristics

For comparison purposes, the table below lists the current capabilities and features of FIERA and IRACE. The requirements for the NGC are detailed on document XXX-XXX-XXX-XXX.



	FIERA	IRACE
Clock voltage range	-14.5V..+14.5V	-10V..+10V
Number of clock lines	14 per board	16 per board (1)
Maximum number of clock boards	4	2
Clock line maximum current	500mA or higher	30mA
Clock voltage accuracy	12-bit	12-bit
Clock multilevel support	YES	NO
Bias voltage range	-15V..+30V	???.???
Number of bias voltages	32 per board	16 per board (1)
Preamp noise	Not measured	???
Preamp gain adjustable	YES	NO
Preamp gain range	1.5 to 3 (adjustable)	3.5 to 8 (Fixed)
Video sample accuracy	16-bit	16-bit
Video sampling frequency (2)	2MS/s (limited by the ADC)	2MS/s (limited by the ADC)
Number of video channel	4 per board	16 per board
Video chain noise (referred to the preamp input)	Not Measured	???
Embedded image processing	YES	NO
Seamless running sequencer	YES	YES
Sequencer granularity	20ns or 25ns	50ns
DMA transfer	PCI 33MHz/32-bit	PCI 33MHz/32-bit
Linearity		
Non-linearity		
Shutter interface	YES	NO
Need of water cooling	YES	NO

(1) Clock board and bias board combined.

Even though both controllers have proven its performance and flexibility in coping with a growing number of new detectors and detector systems, there is a long list of new requirements not currently met neither by FIERA nor IRACE. Some of them are:

- L3Vision: Clock voltages up to +40V and sine wave.
- OTAs and Orthogonal transfer CCDs: Digital interface to address the multiplexor.
- ASIC support.
- Flexible modularity able to be scaled up or shrunk down to our needs.
- Multi-gigabit optical link.
- Fully-fledged on-the-fly image processing.
- Conformable form factor, big and with many channels or small with a few channels and lightweight.

There are however some desirable features encountered in IRACE and not in FIERA and otherwise, e.g. low weight and power consumption (IRACE), high current clock lines (FIERA), no need of water cooling (IRACE), embedded video processing (FIERA)...

3 Controller general block diagram

Figure 3-1 shows a generic block diagram with the functionalities required to read an IR or a visible detector. These functionalities can materialize on specific boards in many different ways and this allocation across the boards can affect the flexibility, modularity and even the performance of the controller.

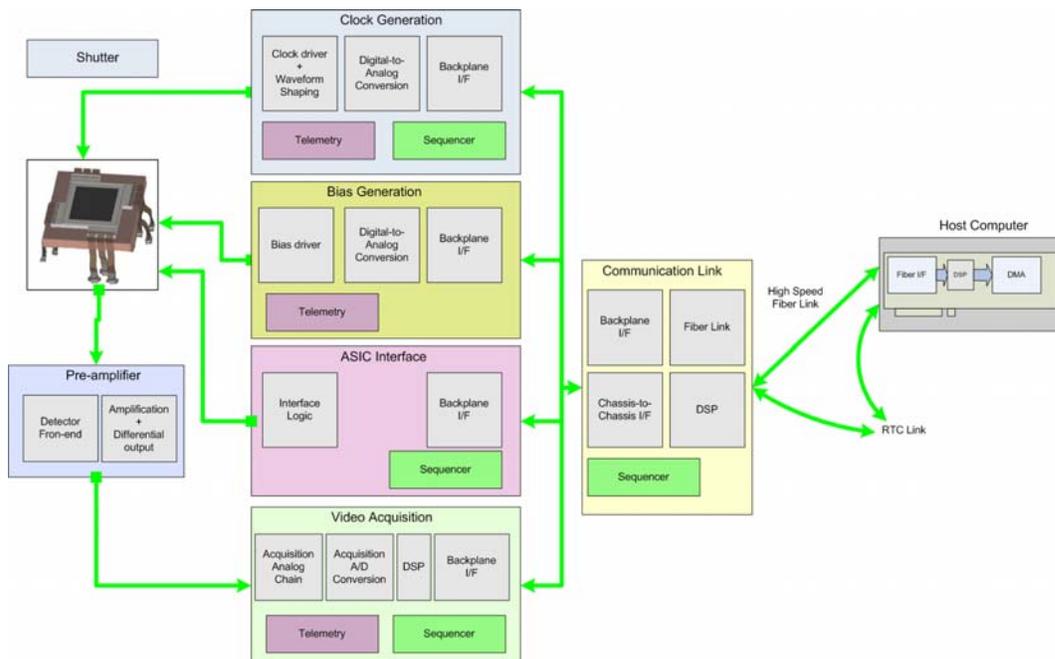


Figure 3-1: Detector controller generic block diagram.



Some functionalities on this diagram are redundant and can be placed on a different place or not placed at all, e.g. DSP block, and some others, e.g. the sequencer, can be shared between blocks.

4 Controller modularity and board partitioning

Concerning modularity, an architectural issue to be addressed is whether or not the boards combine functionalities (i.e. clock and DC voltages generation, video acquisition, sequencer and data communication) and how these functionalities are distributed. The distribution will affect the number of boards that a system will require and therefore its weight, power consumption and cost.

The following list illustrates how different detector controllers have reached different distribution of functionalities:

- FIERA approach (a board per function):
 1. A clock board with on-board sequencer.
 2. A bias board.
 3. A video board with on-board sequencer.
 4. One communication board with on-board sequencer.
- IRACE approach:
 1. A board combining clock and bias voltage generation.
 2. An acquisition board.
 3. A communication/giga board.
 4. A board with the main sequencer.
- Monsoon approach:
 1. A combined clock and bias board without built-in sequencer.
 2. A combined bias and video board for IR without built-in sequencer.
 3. A combined bias and video board for optical detectors without built-in sequencer.
 4. A board combining the communication and main sequencer board.
- Example of any other feasible board partitioning:
 1. One combined clock and bias board and with sequencer.
 2. One video board (no bias generation) and with sequencer.
 5. A communication/Giga board.

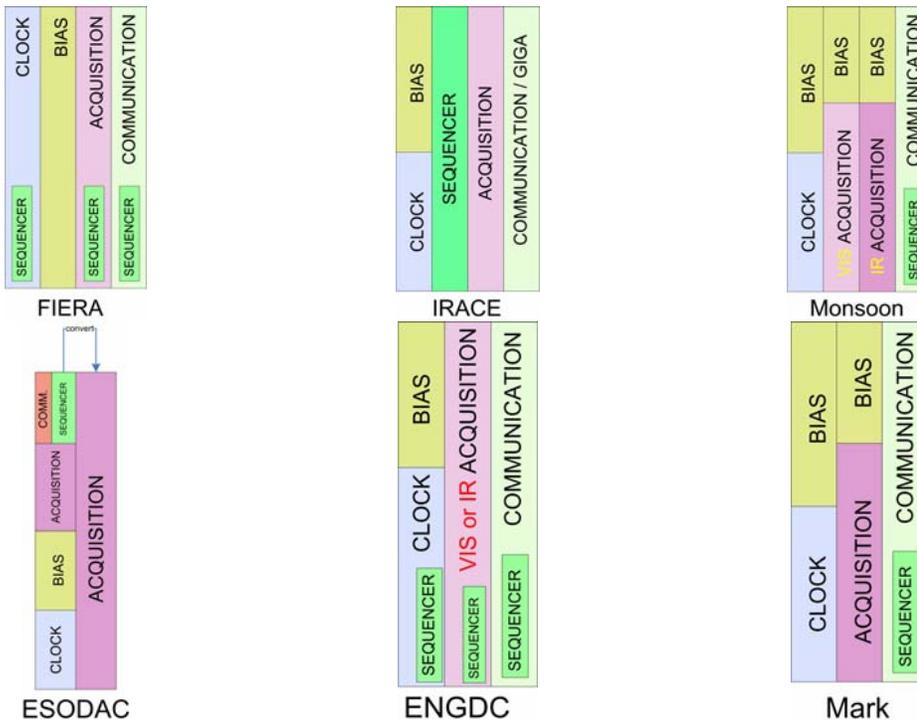
In case of going for boards combining functionalities, one important question would be the relative optimum number of channels a board should contain. This question is of particular

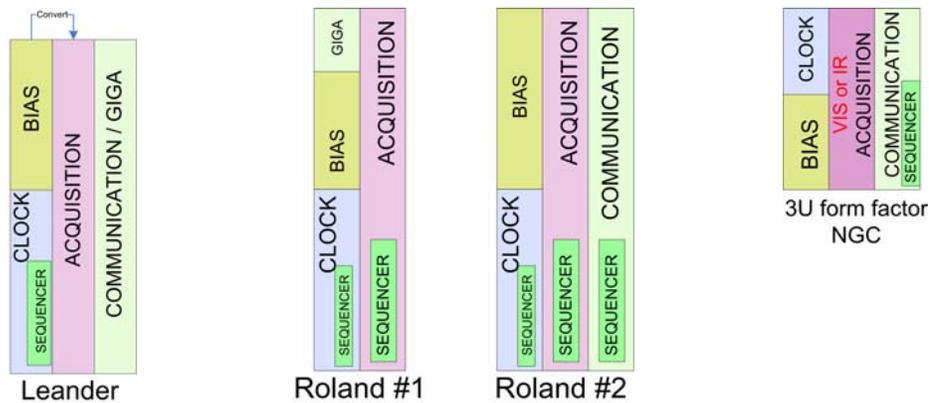
importance as infrared detectors need in general few clock lines and many video channels whereas on optical detectors the situation is reversed.

Apart from the implementation issues detailing how boards on the detector electronics interface to each other, another point of discussion should be whether chassis-to-chassis connection is supported and if so, whether the chaining of detector front-end electronics it is seen by the software on the host computer (back-end in the terminology followed by the IR group) as a single detector electronics with more channels or a just as a collection of independent detector electronics. The way the hardware implements this architectural issue may well have an impact on the way software is structured and instantiates to support either a single detector electronics or an array of them.

4.1 Board partitioning cases

To support the discussion on board partitioning a number of cases are listed below.





4.2 Board partitioning. Local versus centralized sequencer

Concerning the location of the microsequencer the options are either having a central sequencer on one board and pass the control signal thru the backplane to the rest of the boards (IRACE, Monsoon, Mark) or having each board with a local sequencer. Both approaches have pros and cons detailed in the following.

Centralized sequencer:

Pros:

- Real Estate only on one board
- No synchronization issues to be addressed

Cons:

- Signal toggling on the backplane
- Limited number of boards that can be addressed

Local sequencer:

Pros:

- Fast signals do not have to be sent over the bus
- Lower EMI
- More accurate timing (no subjected to backplane delays)
- No limitation on the number of boards

Cons:

- Real estate consumed on each board
- Synchronization issues between boards to be addressed (however the synchronization is limited to proper distribution of clock and start signal)

Discussion on modularity:



- Optimal board partitioning
- Location of the sequencer: Local or centralized

5 ASIC support

As the future prospects are to find an ASIC attached to the detector, we will need to support classical detectors requiring both analog biasing and clocking along with detectors with a built-in ASIC whose interface needs are limited to a digital one.

An ASIC interface, by definition, is meant to ease the electronic needed to read-out the detector so it is sensible to believe that interfacing to an ASIC will be nothing, but, easy. However, the built-in ASIC is still in a premature phase and more and more detectors will emerge without a common standard. For this reason, the architectural discussion brought up here is whether to implement this interface through a separate and dedicated board or through a standard baseline board with additional capabilities, e.g. a modular clock board with additional functionalities. These two approaches are detailed in the following.

5.1 ASIC support through a dedicated board

Figure 5-1 shows the interface through a dedicated board on which the electronics is limited to an ASIC digital interface plus the standard backplane bus interface. From an electronic point of view a board to support ASICs would work as a combined clock board (without the analog part that produces the swinging rails) and an acquisition board (without the analog part), and for this reason, a standard clock board and an acquisition board, provided some modularity on them, could achieve the same than a dedicated board.

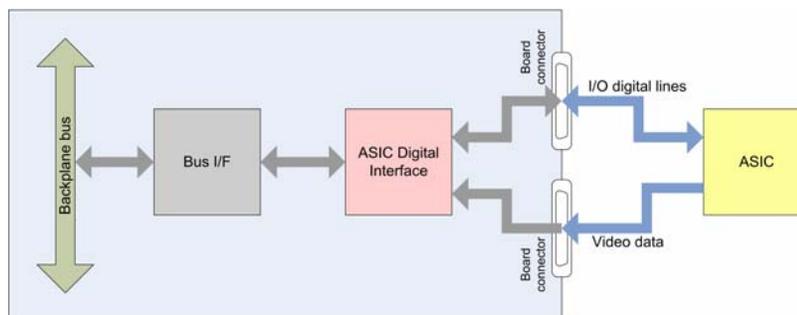


Figure 5-1: ASIC interface via a dedicated board.

5.2 ASIC support through the clock board or clock/acquisition board

The option discussed here is the ASIC support through the same set of baseline boards instead of a dedicated board.

As mentioned on Section 5.1, another option would be to have a modular clock board consisting of a sequencer and the analog part in charged of producing the output swinging rails. Figure 5-2 sketches this implementation. If the analog part of the clock board can be bypassed the remaining part (bus I/F and sequencer) can in principle interface to an ASIC. The dash line in Figure 5-2 represents the video data path which can be through the acquisition board or through the same clock board. (Without having foreknowledge of the ASIC interfaces to come, if the video data path is through the same clock board the digital lines must be bidirectional in order to support some handshake or protocol with the ASIC.)

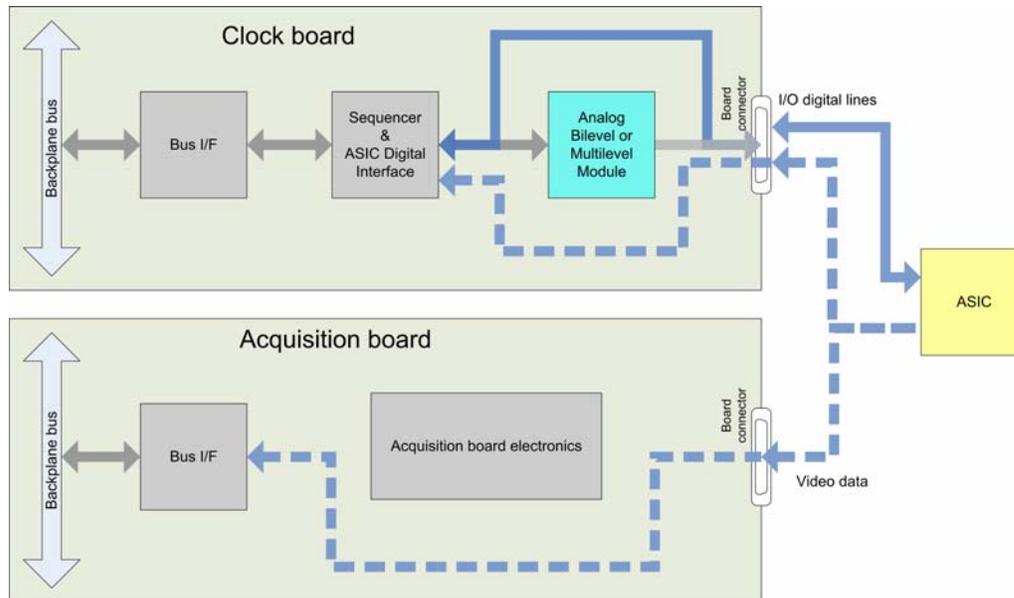


Figure 5-2: Modular clock board to support ASICs and classical focal planes.

Having a modular clock board with its analog part as an add-on module that can be bypassed (or even not plugged or not populated) would have two benefits:

- 1) The analog part can be either a module producing two clock levels or a more complex waveform in order to fine tune the output clock shape (equivalent to FIERA's multilevel waveform shaping).
- 2) The modularity of the clock board and the acquisition board would reduce the number of type of boards to be designed and maintained. In other words, ASIC would be supported as part of the same set of baseline boards.

However the modular approach described here is not exempt from some other disadvantages that should be further discussed.

NOTE in support of a dedicated board for ASIC: ASIC will come but it is still uncertain whether they will converge and have a common interface. It is foreseeable that they will arrive in many varieties, therefore, a dedicated board does not seem bad option

Discussion on ASIC Support of the NGC:

- The support of ASIC can be conceived either via a dedicated board or via standard but

modular board.

- If standard boards are to be used to support focal planes with ASIC the options are:
 - The clock generation board can work with bidirectional lines and it would be the only one involved in the interface.
 - The clock generation board and the acquisition board take care of the interface to ASIC. On the clock generation board the analog part is bypassed, not populated or not plugged. On the acquisition board, only the interface to the backplane is used.

6 Optical link

Currently both FIERA and IRACE use an optical fiber link to connect the front-end electronics to the host computer. On both systems it runs at 1.25Gbps but using different modules from two different manufacturers. See Figure 6-1.

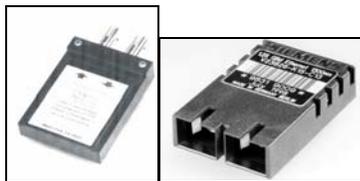


Figure 6-1: FIERA (left) and IRACE (right) 1.25Gbps optical transceiver.

With respect to the optical link from the detector electronics to the host computer, the new generation of infrared detectors seem to be more bandwidth demanding than their forthcoming optical counterparts. For example the requirements of the new Hawaii-2RG detectors is to read a 2kx2k detector every 26 ms which requires (if no processing of raw data is performed on the acquisition board as discussed in Section 13) a 2.46Gbps optical link.

Fortunately, optical transceivers are very mature off-the-shelf modules and very high-speed transceivers can be bought as a black box module. For example, there are in the market modules at 3.125Gbps and reaching lengths of up to 40km (see Figure 6-2) and in the near future it is announced an increase on the speed of up to 10Gbps and a reaching length of 10km with multi-mode fiber and 40km with mono-mode. For this reason, a sensible solution would be to choose the highest speed module available at the design time, e.g. 10Gbps now, for the communication between the detector electronics and host computer in spite of that speed is three times above the most demanding requirement. Needless to say that this excess in the optical link requirement should not imply a substantial higher design cost in time or money.

However, as the network companies are, and will always be, at the forefront of the high-speed optical links requirements, another option that should be discussed is whether to build or to buy the optical module from a manufacturer already producing optical point-to-point fiber links for embedded networking solutions. This idea is not new and is in fact the approach taken by Monsoon in order to save design time and make the system scalable without the need of future redesigns of the point-to-point link.

At a first look at this issue, one of the disadvantages in buying a commercial off-the-shelf (COT) board for the optical link would be its interface to the backplane. If we decide to use a custom or semi-custom backplane for the detector electronics, the possibilities of finding a commercial board which fulfils our optical link requirements, and at the same time is able to interface to our backplane would be very scarce.



Figure 6-2: 3.125Gbps, 10Gbps and 2.5Gbps modules from Finisar.

In this context the IEEE's CMC standard could allow us both to overcome the need of designing such widely used functional block, and at the same time, having a custom backplane. (CMC defines the size of the slave mezzanine cards, the type of connector to be used and the position of the connectors on the master board and on the slave board.) The small form factor of a CMC board makes it ideal for plugging on a 6U or even on a 3U motherboard without increasing the width of the board. See Figure 6-3.

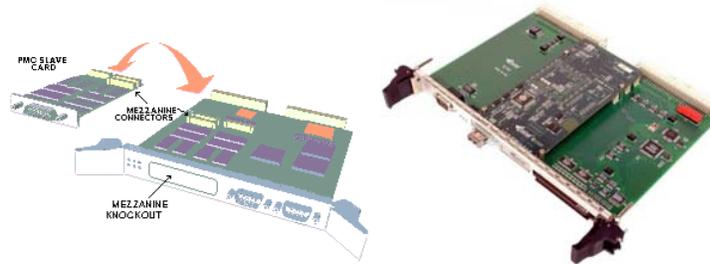


Figure 6-3: CMC Mezzanine board.

6.1 COT boards for optical link between front-end and back-end

Several COT add-in boards have been found in the market for a point-to-point to fiber link at 2.5Gbps (requirement to read a HAWAII-2RG every 26ms). These boards are listed below along with their main features.

6.1.1 S-LINK card

- 2.5Gbps
- Open standard by CERN and available from CERNTECH
- Duplex
- 32-bit data width
- Linux, VxWorks.

See Figure 6-4.

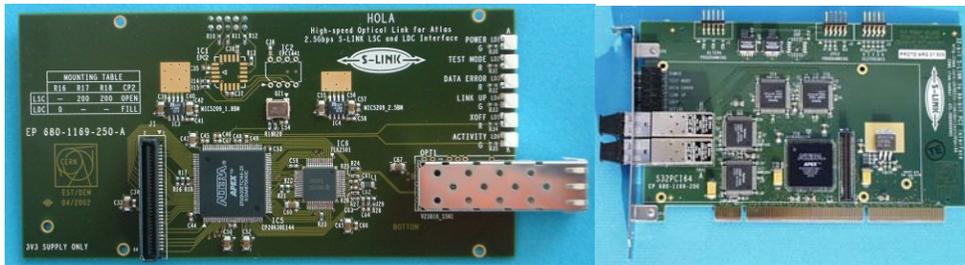


Figure 6-4: CERN HOLA S-LINK board for point-to-point fiber communication.

6.1.2 Multi-point FILAR Card

- Four HOLA S-Link (2.5Gbps) card
- 33/66 and 32/64 PCI interface
- CERN open standard
- Able to communicate to HOLA S-Link board
- Linux, VxWorks.

See Figure 6-5.



Figure 6-5: CERN FILAR multi point fiber card.

6.1.3 Systran FiberXtreme SL240

- 2.5Gbps (10Gbps available in one year)
- 64-bit PCI
- Support HPUX, Solaris, Linux, VxWorks and Windows
- PMC and CMC standards

Figure 6-6 shows some of the boards available by Systran for the fiber communication.

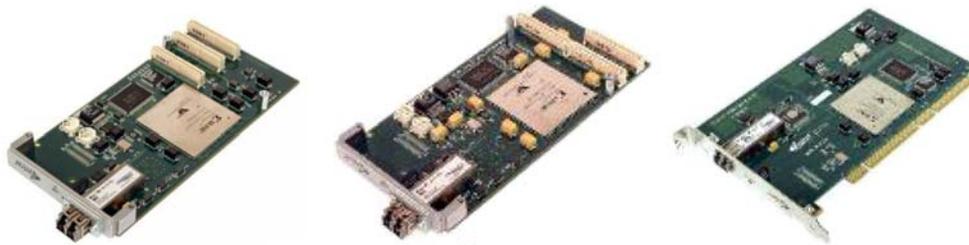


Figure 6-6: CMC, PMC and PCI FibreXtreme cards from Systran.

Discussion on the point-to-point optical link between the front-end and the host computer:

- High-speed point-to-point optical links have become a standard functional block available in the market and at the speed required by the NGC: 2.5Gbps.
- These add-in cards can be plugged both on the host computer motherboard and on the front-end communication board without increasing the board width so their utilisation would not impact the detector electronics size.
- The CMC/PMC standard seems to be suitable for our purposes and some companies selling such boards support Solaris and Linux so software development is reduced to a minimum.
- It seems that the custom design of a point-to-point optical link would be only justifiable if on the host computer, apart from the high-speed optical link, some others functionalities are to be integrated, e.g. RTC interface, external synchronization. However, even in this case, the optical link on the detector front-end can still be a CMC piggy-back board available commercially.

6.2 About the new optical link and the backward compatibility

This section can be overlooked if back-compatibility is not considered as a requirement for the next generation controller.

An issue that may be taken into consideration is the backward compatibility when moving to a higher speed optical link. If back compatibility is of some importance, a solution would be to have this module as pluggable so the interface board on the host computer can communicate either to FIERA, IRACE or the new controller by simply changing this module. Figure 6-7 illustrates this point.



Figure 6-7: Host computer board with piggy-back optical modules.

7 Connection of the detector electronics to the detectors

As it is done in Monsoon, the connection of the detector through the backplane instead than through connectors on the front panel is an attractive idea to be discussed. Even though this idea may sound strange a priori, there are many pros and cons to be assessed. A clear advantage is that with this scheme, the connection to the detector is not limited to the area of the front panel of the board or to the connectors available in the market for such purposes, and therefore, bigger and better connectors, e.g. military, can be used. Figure 7-1 shows the connection between the front-end electronics and the detector as it is on Monsoon. **Even though the figure shows the connection via flex-rigid cable, this solution presents serious disadvantages and is not very attractive. The connection with normal cables is also feasible.** (An intermediate board connecting the back-plane and the connector/connectors on the back-panel would ease the connection.) Figure 7-2 shows a HAWAII-2RG multiplexor connected to Monsoon through the backplane.)

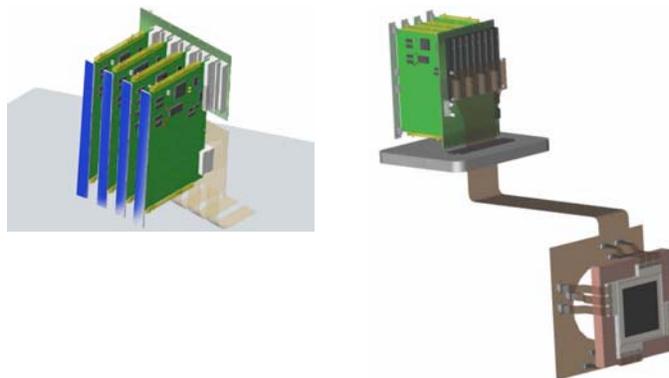


Figure 7-1: Monsoon backplane connection to the detector.

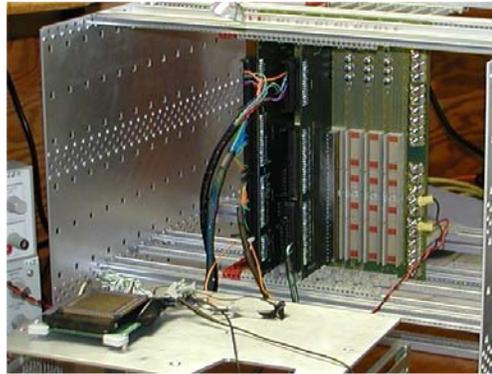


Figure 7-2: HAWAII-2RG multiplexer connected through the backplane of Monsoon.

Discussion on the connection of the detector through the backplane:

Pros:

- Less real estate needed on the PCBs.
- Easier maintenance (boards can be swapped without removing cables).
- Direct connection to the cryostat a la MEGACAM possible.
- No stress on connector solder joints.
- Not to worry about suitable connectors for the front-panel, e.g. MIL type on the back panel.
- A simple bus extender board is a break-up board for test purposes.
- Mechanically robust.

Cons:

- More expensive.
- Board position on the bus fixed.
- Extra design work on flex-rigid PCBs needed.
- EMI needs to be addressed.

8 Boards form factor

Although the chosen form factor both on FIERA and IRACE is 6U, it would be worth to investigate if it is feasible to define the architecture in such a way that it allows the front-end detector electronics to be made either with 6U or 3U form factor boards. See Figure 8-1. By doing this, huge and spread instruments like MUSE would be much more easily covered. This flexibility in the form factor seems to have certain advantages on sensing application systems, i.e. AO and ancillary systems. (This flexibility in the form factor would also serve Technical CCDs even though these systems are out of the ambitions of the NGC.)

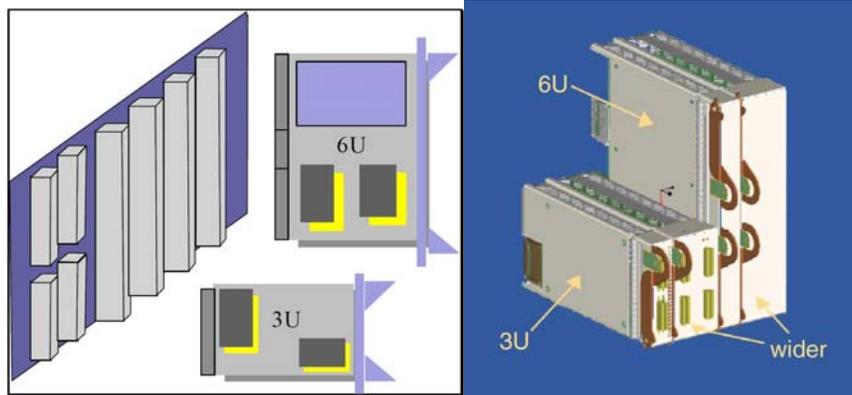


Figure 8-1: 6U and 3U form factor.

This idea is partly induced by the CompactPCI specification on which the boards can be either 6U or 3U. Some way to achieve this could be to design the boards symmetrical, e.g. a 6U acquisition board with 16-channel would contain 8 channels on the upper part of the board and 8 channels and the common logic on the lower part. A more elaborate solution is presented in Section 10 in connection with Serial Switched Fabrics backplanes.

9 Backplane and backplane bus

Even though the use of a custom backplane in FIERA and IRACE reports some benefits, it is true that having a custom defined backplane always blocks the option of using commercial off-the-shelf boards either as part of the detector electronics or for ancillary functions. On the other hand, a legacy bus can be adapted closely to our needs and there is a peak performance gain. Because of this dichotomy, it would be worth to investigate and look what other scientific communities has found as a solution for a similar problem.

Some options worth to be discussed and in principle able to fulfil our requirements without falling in pitfalls of the past might be:

- Fully standard electrically and mechanical CompactPCI (cPCI).
- Serial Switch Fabrics. Point to point serial bus based on Compact PCI mechanical form factors.

(Although VME has evolved over time to support up to 64 bits bus size and is undoubtedly a solid technology it is not considered here because it has become dated.)

9.1 Fully compliant CompactPCI bus

That would require PCI bus bridging on every board. Some of the advantage would be:

- PCI-to-Local bus bridging is inexpensive and has a small footprint.

- PCI-to-Local bus bridging is a well-known technology by the Infrared and the ODT groups.
- Fully compliant PCI bus on-board would ease board debugging as commercial board can be used for testing purposes.
- Clear and well documented bus interface to peripherals that would ease task distribution among people in both groups.
- Mature PCI-to-PCI bridge to perform chassis-to-chassis interconnection and chain detector electronics whenever is needed.
- Many commercial boards available in the market.
- Possibility of putting the bus to idle while integration to improve noise performance.

Some of the disadvantages are:

- PCI 32/33 may not have enough throughput for our application.
- Non-deterministic.
- Bus time overhead on a master/slave devices on requesting the bus.
- High pin count need in comparison with high-speed serial buses.
- EMI problems associated with parallel buses.

9.2 Point-to-Point high-speed serial bus. Serial Switched Fabrics.

This is a new trend in telecommunication systems and very demanding industrial embedded electronics. It is a very attractive solution that solves many of the problem of parallel buses. It consists in funnelling parallel data through a differential high-speed serial bus, e.g. nominal speed of 3.125Gbps on the Virtex-II family from Xilinx. See Figure 9-1.

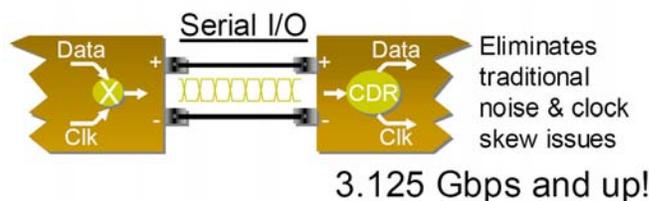


Figure 9-1: Serial Switch Fabrics.

The advantage of this type of bus would be:

- Very high throughput. Three complete PCI buses can be funnelled through a single link.
- Very flexible board-to-board communication possible.
- Very reduced pin/trace count so many more pins on the backplane can be used for custom signals.
- No clock skew as clock is embedded in the data.
- Chassis-to-chassis interconnection possible to chain detector electronics if required.
- New upcoming standards (InfiniBand, RapidIO, 3GIO, StarFabric...)
- Low voltage differential.
- Low power.



- Point-to-point board communication possible.
- Highly scalable system: 1 to 40Gbps by link aggregation.
- There are indications of success on running this type of bus on standard CompactPCI backplanes.
- EMI issues might be easily solved.

The disadvantages are:

- New technology and high-speed design challenges.
- Expensive design tools.
- EMI to be assessed as high frequency signal might not be so easily filtered.

It is believed that the benefits of a Serial Switch Fabrics bus can be exploited to attain a 3U form factor front-end electronics with no impact on performance or other requirements.

9.3 Some notes in support of a CompactPCI backplane mechanical standard

Both FIERA and IRACE use a custom backplane similar to the VME-backplane from its dimensions, slot distance, and power pin assignment. Because of the compatible mechanics and ground/power pin assignment, standard VME-extender boards have been used for testing purposes. However, the bus needs active termination on both ends and it consumes power.

CompactPCI merges the electrical and software standards of the PCI bus with the Eurocard format and high density 2-mm pin and socket connector. The Eurocard mechanical structure of CompactPCI is the same format popularized by VME, which eases system integration and servicing of PCI I/O boards in the system.

CompactPCI boards use a high-quality 2mm pin and socket connector that meets industrial and telecom standards. These connectors are very reliable and provide better shock and vibration characteristics than the card edge connectors of standard VME bus. Eurocard 3U and 6U CompactPCI boards are inserted from the front of the system, and I/O can be brought out either from the front or the rear. Like VME, the cards are mounted vertically allowing for convection or forced air cooling.

One difference is the technologies used by the two buses. VME bus is based on a transmission lines with low impedance and both ends of the bus are terminated which imposes a requirement for high-current drivers for most of the signals. However, the CompactPCI bus was designed around the electrical characteristics of CMOS circuitry. This means most ASIC technologies can drive the PCI signal lines directly. Like PCI, the CompactPCI bus design is based on reflected wave signaling instead of incident wave signaling.

As previously mentioned in Section 8, CompactPCI mechanical standard also allows 3U form factor boards in order to have a small controller. Additionally, even though a fully compliant CompactPCI bus is limited to 8 slots, the use a Serial Switched Fabrics bus would overcome such a limitation.

Discussion on the backplane and backplane bus:

- Fully standard or customized backplane (the preference is clearly toward having a customized backplane)



- CompactPCI mechanical standard or VME mechanical standard
- Parallel bus or Serial Switched Fabrics

9.4 Notes on the PCI bus obsolescence and PCI-Express

For the last 10 years the PCI bus has served us well and it is expected to play a major role in the next few years. However, today's and tomorrow's processors and I/O devices are demanding much higher I/O bandwidth than PCI 2.2 or PCI-X can deliver and there is a new generation of PCI, called PCI Express or 3GIO, to serve as a standard I/O bus for future generation platforms.

The PCI Express Architecture meets all of the requirements of a third generation I/O bus. A PCI Express link is implemented using multiple, point-to-point connections called lanes and multiple lanes can be used to create an I/O interconnect whose bandwidth is linearly scalable. The run-time software model supported by PCI is maintained within the PCI Express Architecture which will enable all existing software to execute unchanged and *PCI Express is software compatible with all existing PCI-based software to enable smooth integration within future systems.*

10 On the feasibility of a 3U form factor front-end electronics

For small detector systems where only a few signal are needed, having a front-end electronics based on a 3U form factor does not seem to have an impact on cost, serviceability, testability or performance but it would certainly improve weight, flexibility and modularity. There is of course an electronic space inefficiency in having boards only with 3U form factor in comparison to the 6U boards because they all must contain the digital electronics to interface to the bus. Therefore a 3U form factor board can have less than a half the number of channels a 6U board could have.

The idea of having a 3U form factor is mainly induced by the versatility of Serial Switched Fabrics buses (discussed on Section 9.2), the possibility of having the detector connected through the backplane and the use of CompactPCI mechanical standard for the backplane. If these three conditions are met, the architecture of the NGC can easily be articulated to be consisting of 6U or 3U boards.

The Serial Switched Fabrics communication among boards can be done either through the backplane or through copper lines through the front panel. The former would be a better solution provided that the high-speed digital signals do not degrade the analog ones due to radiated or coupled interference (crosstalk). The connection of board via the front-panel, although less attractive, would in principle alleviate the interference problem. See Figure 10-1.

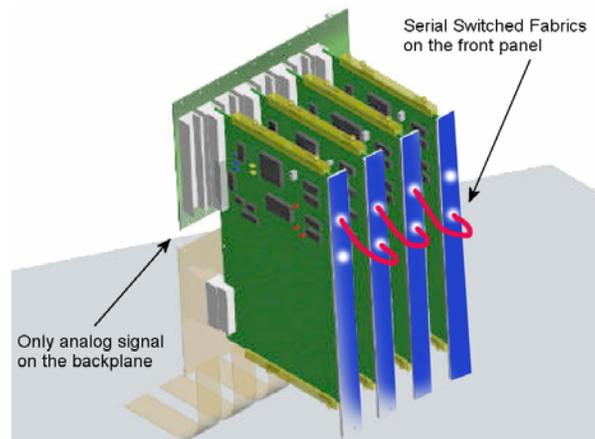


Figure 10-1: Serial Switched Fabric signals on the front-panel.

Discussion on 3U and 6U conformable NGC:

- Can the architecture be designed in such a way that it allows two type of chassis: 6U and 3U ?
- 6U and 3U chassis: Would it be advantageous for very distributed scientific systems (MUSE) or sensing applications ?

11 NGC topology in the context of Serial Switched Fabrics

In Section 10 it is mentioned that it would be advantageous to have front-end electronics that can be made of either 6U or 3U boards. This flexibility in the architecture is feasible mainly to the versatility of the Serial Switched Fabrics, which permits very high-speed board-to-board communication with extremely low pin count (usually 2 or 4 wires). (In the same context, Serial Switched Fabrics would allow the chassis-to-chassis communication.) However, the modularity and ability to scale up or down the front-end electronics depends strongly on the topology chosen for the board-to-board communication.

In general terms and from a data throughput point of view, clock, bias and acquisition board/functionality require more or less the same amount of incoming data for its configuration, housekeeping, telemetry and normal operation. The acquisition board would however require a much higher data rate for its outgoing link to the communication board. On the other hand, the communication board is collecting all the pixels from all the acquisition boards and therefore, its requirement for the incoming data rate is at least N times the outgoing data rate of an acquisition board, where N is the number of acquisition board on the front-end.

The multi-gigabit links have nowadays an easy implementation with the Virtex-II Pro family from Xilinx. On these FPGAs the number of high-speed duplex transceivers on the XC2VP4 and XC2VP7 is either 4 or 8 for respectively. Therefore in the discussion that follows below, the number of transceivers to be employed is a limited resource to keep an eye on. (Xilinx has FPGAs however chips with up to 24 duplex transceivers but these are costly and with a extremely small pitch footprint.)



Some basic topologies are: star, mesh or chain; however an example of hybrid topology is also brought into discussion.

A star topology would allow a point-to-point communication from the communication board to any other board on the system. The star topology is illustrated in Figure 11-1. This topology can cope with the outgoing data stream generated by the acquisition board but, using a high-speed transceiver for the communication between the communication board and the clock and bias boards would certainly be a waste of bandwidth. On the other hand, a star topology would consume all the communication channels of the communication board but only one duplex channel on the rest of the boards (it would take only one channel if no channel aggregation is made). Additionally, a start topology would limit the number of boards of the front-end electronics to the number of transceivers in the chip we use to implement the serial communication. (In the case of the XC2VP7 the number of boards would be limited to 8.)

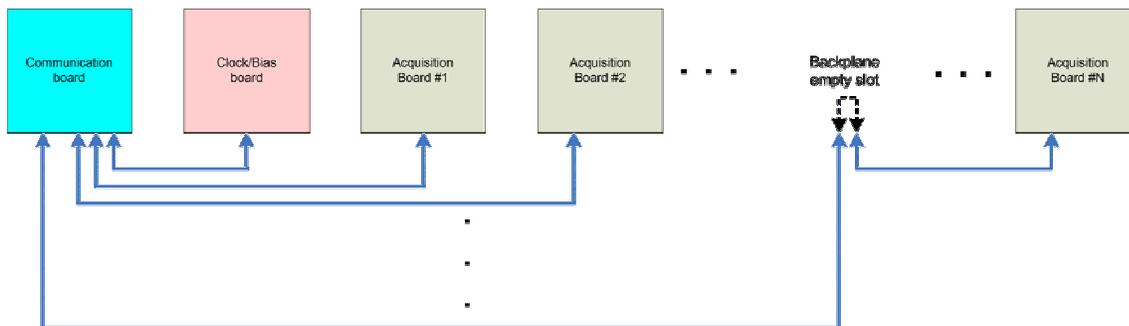


Figure 11-1: NGC board-to-board star topology.

A mesh topology would consist of a communication channel from each board to any other on the front-end. See Figure 11-2. These topology does not seem to present any clear benefit for our purposes for various reasons. For example, the links between acquisition boards or between acquisition boards and clock/bias board are useless.

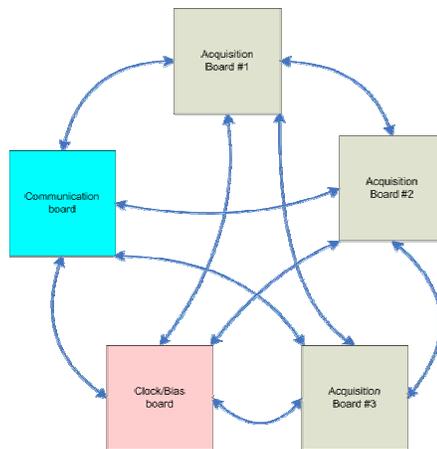


Figure 11-2: NGC board-to-board mesh topology.

A chain topology is depicted in Figure 11-3. This topology would require only two communication transceivers and is clearly unsuitable to transmit the outgoing video data from the acquisition board to the communication board. As seen on the bottom of the same figure, in the case of basing the architecture on duplex transceivers, the acquisition board N needs to pass its video data on to board N-1, and, acquisition board N-1 needs to combine the video data from board N and its own outgoing video data and pass it on to acquisition board N-2. The situation is not dissimilar when using simplex transceivers. However, this topology would be suitable for configuration, telemetry purposes and control operation during read-out, e.g. updating/refresing on-the-flight the microsequencer parameters.

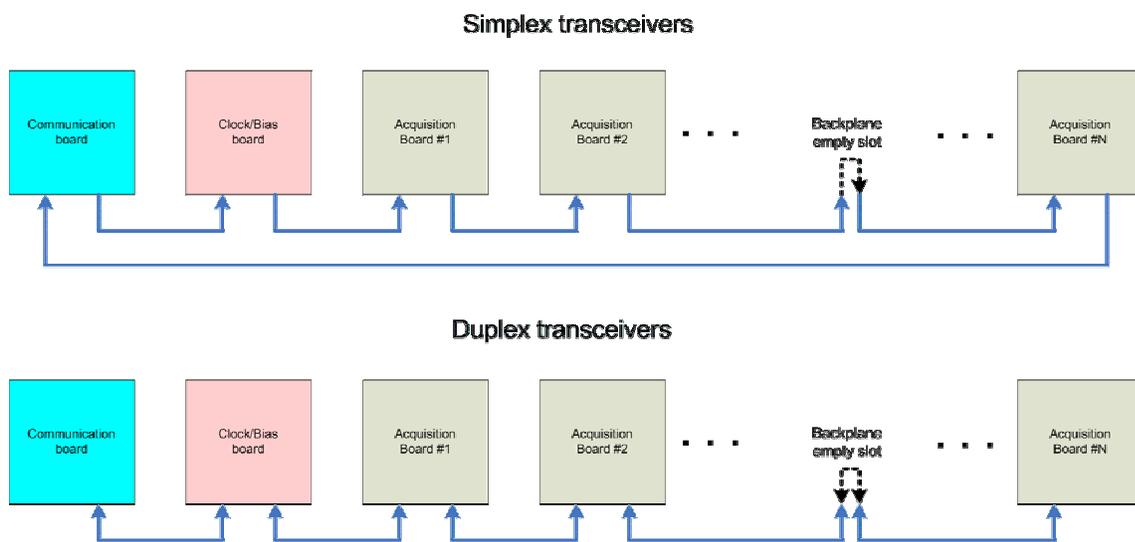


Figure 11-3: NGC board-to-board chain topology.

Having said that the requirements for the incoming and outgoing data rate depends on the type of board into consideration, a hybrid topology can better be pursued. The figure below shows an example of hybrid topology wherein boards are chained together to conform a bus for configuration, telemetry and board control, and a simplex dedicated multi-gigabit links are used for the transmission of pixel data from each acquisition board to the communication board.

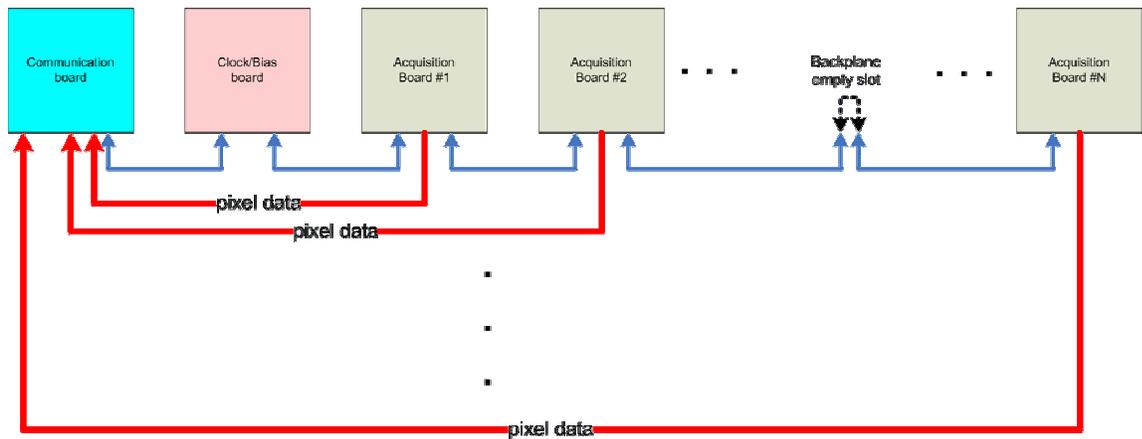


Figure 4: NGC board-to-board hybrid topology.

In case of using SSF for the board-to-board communication, the variety of hybrid topologies is very high and the scalability of NGC will depend very much on the type of topology chosen.

For illustration purposes, Figure 11-5 shows a NGC based on a star topology. Some photos of such a hypothetical controller are shown in Figure 11-6 and Figure 11-7.

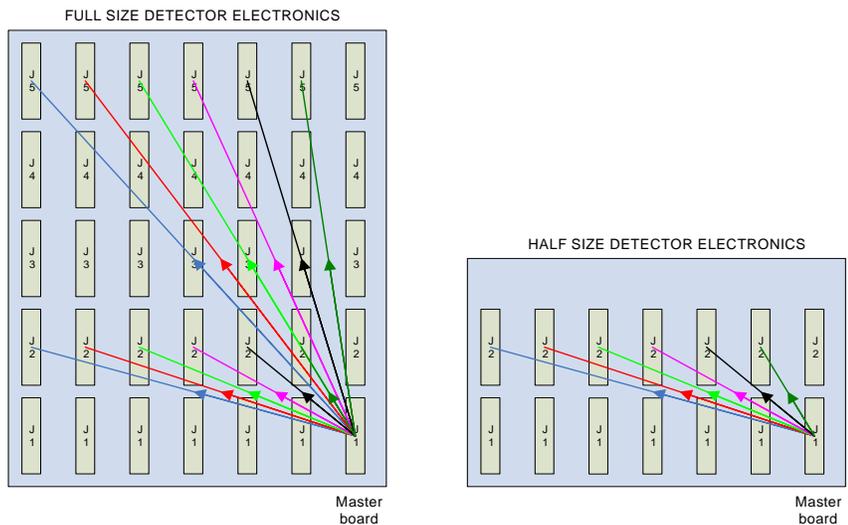


Figure 11-5: 6U and 3U DCE implementation based on Serial Switched Fabrics.

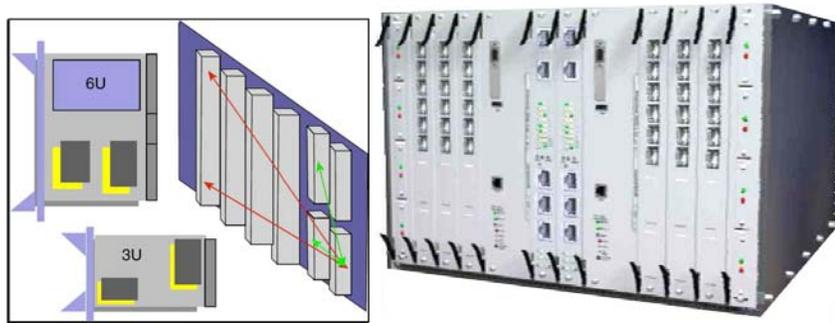


Figure 11-6: Hypothetical system extended horizontally to support bigger focal planes.



Figure 11-7: Hypothetical NGC system with 3U form factor.

In addition to the board-to-board communication, a serial bus with these characteristics allows the chassis-to-chassis interconnection in order to scale up the detector electronics whenever is needed. This chassis-to-chassis connection could be done in such a way that, from the host computer side, the control software sees a single detector electronics but with many more channels.

11.1 Some standard serial buses

There are several standards in the market based on SSF, these are: InfiniBand, RapidIO, HyperTransport, StarFabric and 3GIO (also known as PCI-Express). Some of the characteristics of these standards are compiled in Table 1.

	InfiniBand	RapidIO	HyperTransport	StarFabric	3GIO
Chip-to-chip	???	YES	YES	???	NO
Board-to-board	YES	NO	NO	YES	YES
Chassis-to-chassis	YES	NO	NO	YES	YES
Xilinx IP support	???	YES	YES	YES	NO

Table 1: Some standards based on Serial Switched Fabrics.

Not all these standards are suitable for our purposes but it would be interesting to investigate whether the multi-gigabit serial bus for the NGC can be based on some of these standards in order to use, if possible, COT boards for the communication boards.

Discussion on the topology of the NGC serial bus:

- The basic topologies are: star, chain, mesh.
- None of the basic topologies seem to satisfy the requirements in terms either of scalability or data throughput.
- A hybrid topology seems to be a good trade-off of scalability and data throughput.
- Huge variety of possible hybrid topologies. Which one is best for our application ?
- What are the options for the chassis-to-chassis connection?

12 Analog Video chain

The electronic chain both on FIERA and IRACE consists of a preamplifier (either integrated in the cryostat or external to it), a differential video cable and the video acquisition board (AQ in IRACE terminology and Video board in FIERA).

12.1 Preamplifier Differences

The main differences between the preamplifier in FIERA and IRACE are the type of coupling to the detector, AC in FIERA and DC in IRACE; and the gain at which they operate, adjustable in FIERA and fixed in IRACE. Moreover the preamp of FIERA has a current source on the video input to sink a constant current from the output transistor of the CCD. This constant current source is employed on E2V CCDs and not populated for the MIT. The following lines further comment on these differences.

12.1.1 Preamplifier coupling. AC- vs. DC-coupled

The video output of a CCD has usually a low dynamic range, e.g. 70mV for E2V chips and 700mV for a MIT, and is mounted on a high voltage offset. (Figure 12-1 shows a typical video output signal from an E2V chip.) Therefore, for CCD applications, the preamplifier needs to be AC coupled from the incoming video signal. However on an IR detector the video output is DC coupled in order to subtract the reference pixel offset right at this first stage of amplification.

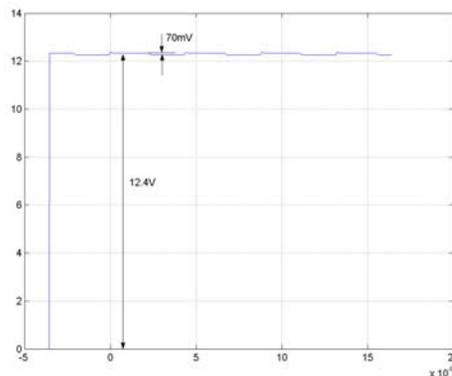


Figure 12-1: Typical video output from a CCD (E2V).

12.1.2 Preamplifier gain

Contrary to the preamplifier used in IRACE, which operate at a fixed gain, the preamp in FIERA has an adjustable gain of 1.5, 2.25 and 3. However, the gain on the preamplifier is almost always fixed to 2.25 and we prefer to amplify the signal on the video board where we also have a programmable gain amplifier. Therefore, this difference between the two preamps is in practice minimal. Nonetheless, there may be CCD systems already deployed (I don't know if it has to be considered) which modify both with the gain on the preamp and the video board in order to trim the final gain of the video chain. For backward compatibility purposes, this might be an issue to keep in mind.

The magnitude of the gain on the preamps on IRACE and FIERA is comparable and ranging from 3.5 to 8 in IRACE and from 1.5 to 3 in FIERA. The schematics of both preamplifiers are detailed in Figure 12-2 and Figure 12-3.

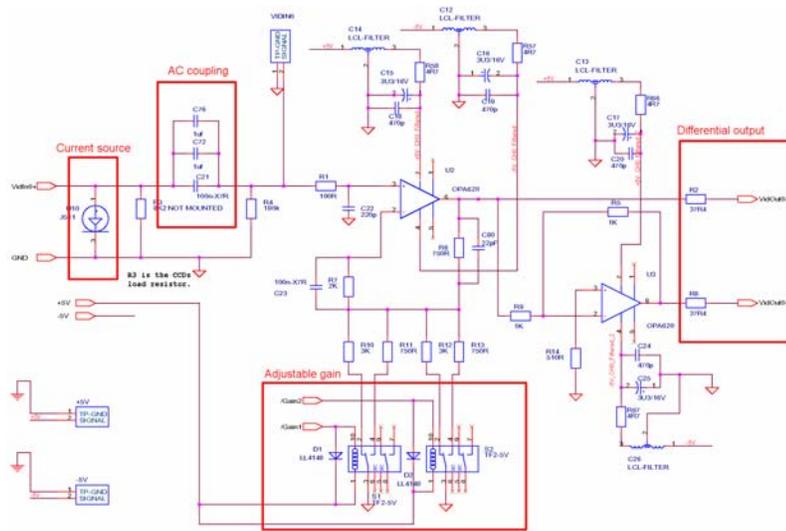


Figure 12-2: FIERA preamplifier. AC coupled and adjustable gain from 1.5 to 3.

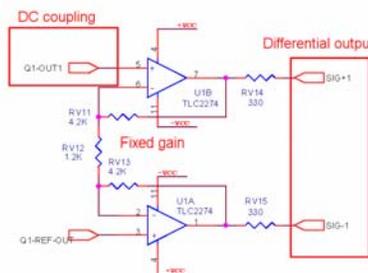


Figure 12-3: IRACE preamplifier. DC coupled and gain of 4.5.

12.1.3 Other preamplifier differences between FIERA and IRACE



Contrary to the preamps in IRACE, which are to work at cryogenic temperatures, the preamp in FIERA does not need to be inside the cryostat and this fact eases its mechanical design. An external preamp implies a higher sensitivity to external ambient temperature and thus variability in the total conversion factor, however, our experience has shown that these variations are negligible and it is not worth to take an action to thermally stabilize the preamp.

Discussion on the preamplifier commonality

- The difference between AC- and DC- coupled preamplifier stages is of no importance to reach commonality.
- Though FIERA preamplifier has an adjustable gain, in practice this gain is never changed and remains almost always fixed. The gain is usually changed on the video board where two modes, basically low- and high-gain, are selected.
- The fact that infrared systems have the preamp inside the cryostat and therefore it needs to fulfil a more restricted mechanical design may hinder the total commonality.

12.2 Video board (FIERA) Acquisition board (IRACE)

From the data acquisition board point of view, IRACE resorts to direct sampling of the input video signal and the processing in the digital domain, e.g. co-adding, regressional fit, Fowler sampling, whereas FIERA, previously to the sampling of the video signal, has an amplifier with selectable gain, a low-pass filter bank with selectable time constant and an analog clamp-and-sample circuit. (The additional circuitry per channel is one of the main reasons why the number of video channels in FIERA is less than in IRACE.) These differences seem to impact the desirable commonality between both video chains.

As mentioned above, IRACE acquisition board has a fixed gain whereas FIERA video board features a selectable gain: low and high. (It is also true that IRACE has also an acquisition board featuring adjustable gain but this is not the one regularly deployed.) This feature is of vital importance for CCD read-out systems and must be maintained as it is used on instruments which has for example an image mode (low gain in order to have higher dynamic range at expenses of worse noise performance) and spectroscopic mode (higher gain to achieve better read-out noise at expenses of lower dynamic range).

From an electronic design point of view and always with commonality in mind, a more profound difference is that FIERA has a configurable set of low pass filter to limit the bandwidth of the video signal and reduce the noise (the optimum time constant for the filter is between 3τ and 4τ) whereas IRACE has a fixed low pass filtered on the video signal path. This selectable filter bank on FIERA plays a fundamental role in the CCD optimization phase and therefore cannot be overlooked. The need for a selectable low pass filter stems from the need of reading the CCD at different speeds in the usual compromise between read-out time and read-out noise. (As an example, up to now the ODT has delivered CCD systems with read-out speed of 50kpx/s, 225kpx/s and 625kpx/s which means that the faster and slower low pass filter must have a ratio 12.5:1 in order to fully optimize the read-out noise.)

Another difference between both acquisition boards resides in the clamp-and-sample circuitry of FIERA. This circuitry carries out the subtraction of the reference from the pixel value in an

analog way. However, although FIERA currently uses analog clamp-and-sample, there are indications that digital CDS, i.e. direct sampling/oversampling followed by digital filtering, would perform as good as or better than its analog counterpart. Therefore, analog clamp-and-sample on the video board of FIERA, which accounts for 26% of the board space, could be saved.

Because of the differences described above, namely adjustable gain, adjustable low pass filtering stage and analog clamp-and-sample circuitry, it would be challenging to design a common acquisition board which supports both IR and CCDs, and at the same time, is able to integrate a big number of channels as required for IR detectors.

See on Figure 12-4 and a Figure 12-5 an illustration of both video chains.

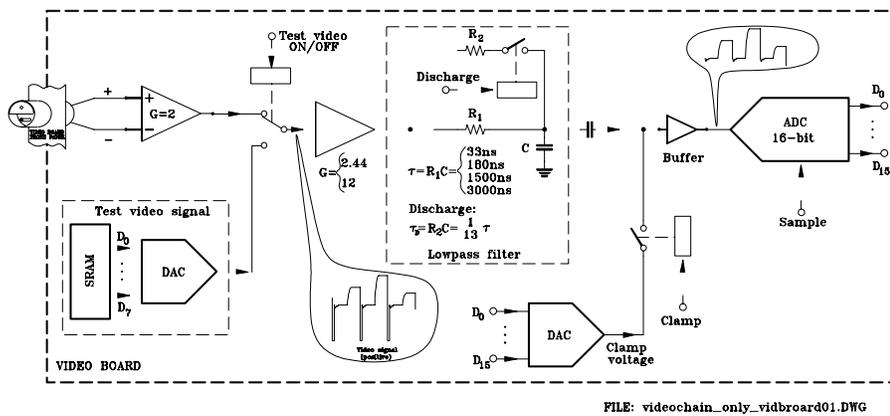


Figure 12-4: FIERA video board analog chain

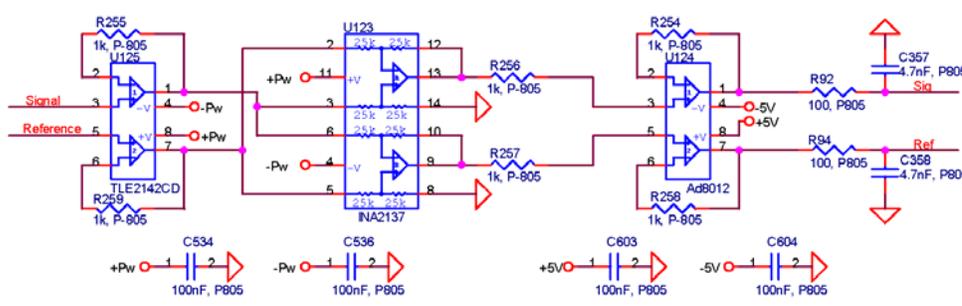


Figure 12-5: IRACE acquisition board analog chain.



Discussion on the video acquisition board commonality:

- With commonality in mind, there exist differences in the analog chain of FIERA and IRACE that cannot be neglected without analysis, namely selectable gain and low pass filter and analog clamp-and-sample.
- If the analog clamp-and-sample is to be removed from FIERA video acquisition chain, a study is needed to demonstrate that 16-bit signal oversampling followed by digital signal processing performs as good as analog CDS.
- At first sight, it seems to be difficult to have a common acquisition board which on the one hand has a high number of channels for infrared focal planes and on the other hand has all the features needed to address CCDs detectors. Therefore, it seems reasonable to have a different acquisition board for visual and infrared detectors. (It is out of question that both boards should have exactly the same digital part.)

13 Embedded real-time image/video processing

First off, three concepts to be distinguished:

- Real-time vs. no real-time.
- Embedded vs. no-embedded.
- Image processing and video processing.

Embedded: Processing that happens on the controller and not on the memory of back-end computer.

Real-time: Data must be processed with a certain bandwidth to control other subsystem, e.g. AO applications.

Image processing: Processing of a complete image and not individual pixels. To do image processing at least one frame needs to be stored in memory.

Video processing: Processing of individual pixels or a set of pixels. To do video processing there is no need to store a complete frame in memory. (NOTE: Video processing is only possible in real-time.)

Digital signal processing: Either image or video processing.

This section is both about embedded real-time image processing and embedded real-time video processing.

In a general context, some situations can be easily foreseen where the incoming video data rate is higher than the data throughput of bus on the back-end computer. By having embedded real-time processing, some raw processing like follow-up the ramp in the infrared or even windowing and centroiding on CCDs, can be done on a DSP (the DSP acronym is used both to

refer to DSPs or FPGAs with DSP functionalities) and only semi-raw or a final scientific image data is transferred to the host computer.

As discussed in Section 12.2, there are reasons to believe that the analog clamp-and-sample performs better than a simple sampling and subtraction in the digital domain, especially when the digital clamp-and-sample consists of a simple subtraction of the video level and the reference level. However, it is believed that oversampling followed by a more sophisticated video processing would perform as good as or better than analog CDS, with the additional benefit of reducing board space in about a 25%. See Figure 13-1.

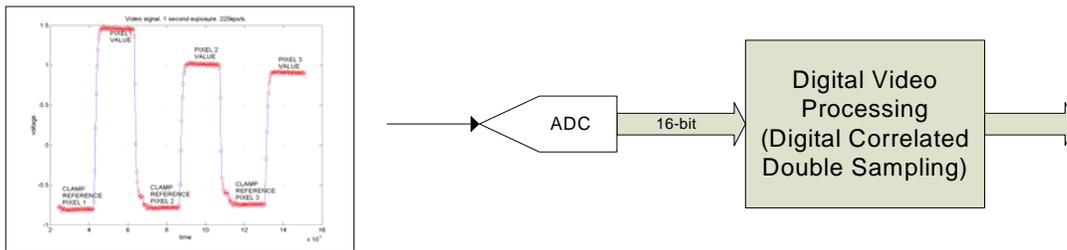


Figure 13-1: Oversampling and digital processing.

13.1 Possible architectures to implement digital signal processing

One aspect of the whole digital processing architecture to be discussed is where to place the DSP or DSPs. If the processing is done on the acquisition board in order to minimize the data sent via the optical link, we are using up space on the PCB that could be used to accommodate more video channels. This architecture is shown in Figure 13-2 and Figure 13-3. However, if the data processing is placed on the host computer side, we may have to restrict the amount of processing power because there is no DSP able to process in real-time all the data coming from the foreseeable detector electronics. This architecture is shown in Figure 13-4.

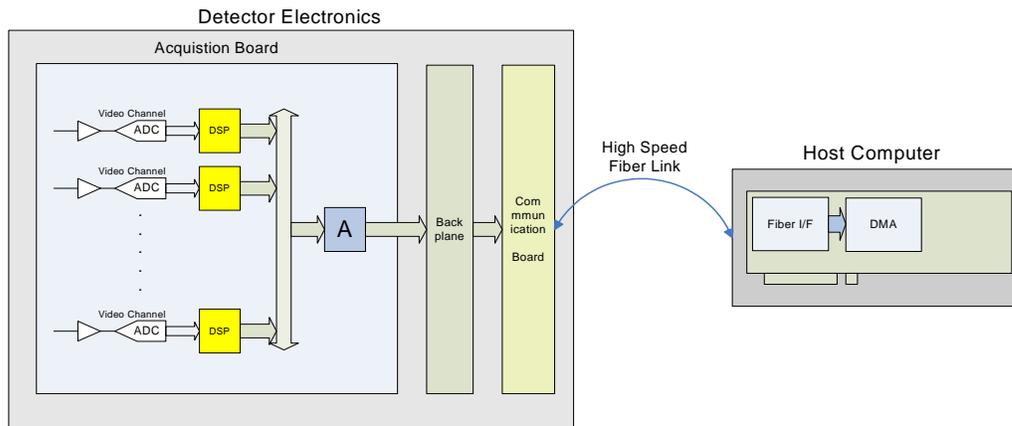


Figure 13-2: On-board pixel data processing. Option 1.

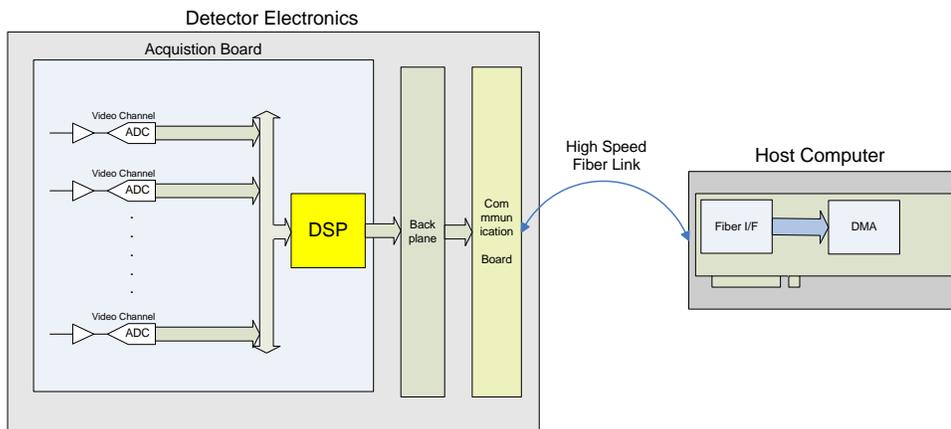


Figure 13-3: On-board pixel data processing. Option 2.

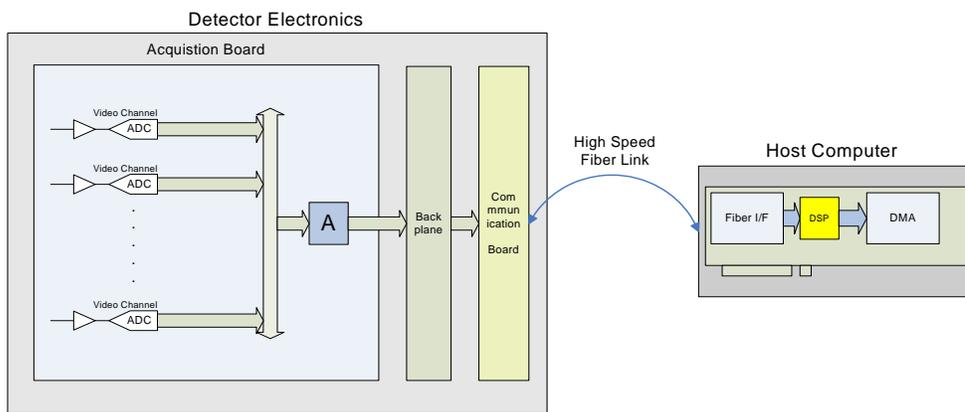


Figure 13-4: Pixel data processing on host interface board.

For the same reasons that the point-to-point optical link can be an COT add-in card (see Section 6), the DSP functionality can also be a piggy-back board plugged onto our acquisition board. Again, the PMC/CMC standard is very suitable for our purposes.



Mango Seagull
4 x 5760 MIPS = 23040 MIPS !!!

Figure 13-5: Mango Seagull DSP module with 4 TI DSPs.

The optical link and the DSP module can be based on a CMC add-in card and the interface to the backplane can be based on the high-speed links of a the Xilinx Virtex-II Pro FPGA. If the DSP module is not be used, it can be bypassed. Figure 13-6 shows the block diagram of the communication board.

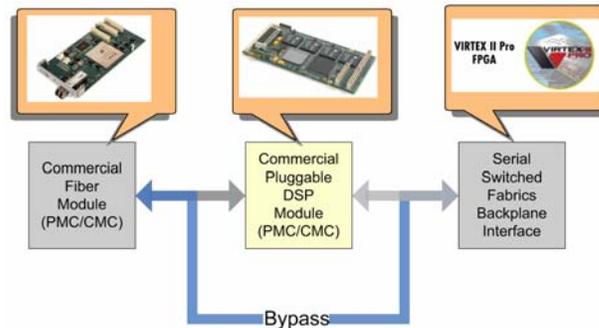


Figure 13-6: Communication board block diagram.

13.2 On an Image Server standard

If embedded real-time processing implementation moves forward, the hardware would do something more than sampling pixels and putting them into the computer memory. The hardware would actually breed an intermediate image to be passed to a higher level software. If this is the case, the hardware (actually the software running on the embedded hardware to be more precise) could be thought as a fully-fledge low-level software layer delivering images to an upper level layer, and we may need to discuss, as Monsoon has a pixel server, if we need something like an image server.

Discussion on the embedded real-time image/video processing:

- What are the requirements for the embedded real-time video processing?
- What are the requirements for the embedded real-time image processing?
- Is there any need for an Image Server standard ?

14 Interface to a Real Time Computer (RTC)

On some applications both IR and visible systems require to pass the image to an external RTC, e.g. CCD systems for Adaptive Optics like NAOS and MAD. The communication interface has been commonly a 32-bit wide word plus some strobe and control signals for the handshake. However, this is a *de facto* interface with no standard to support it, e.g. the interface of FIERA to NAOS and MAD is similar but not the same.

Another common requirement on systems using communicating to an RTC is the need to visualize the incoming video data. This feature may become vital during the alignment and optimization phase in sensing applications.

Discussion on the interface to the RTC:

- To avoid or minimize the need to develop custom interfaces to new flavours of RTCs, we need to define a standard to a generic RTC.
- On systems with an RTC, the back-end needs to support the visualization of the pixel data in order to support the calibration and the optimization phase.

15 Common PCI board visible/infrared

There is no doubt that the board on the host computer (currently called PCI-Giga in IRACE and PCI board in FIERA) can be totally equal.

The block diagrams of a PCI board on IRACE and FIERA are shown in Figure 15-1 and Figure 15-2 respectively.

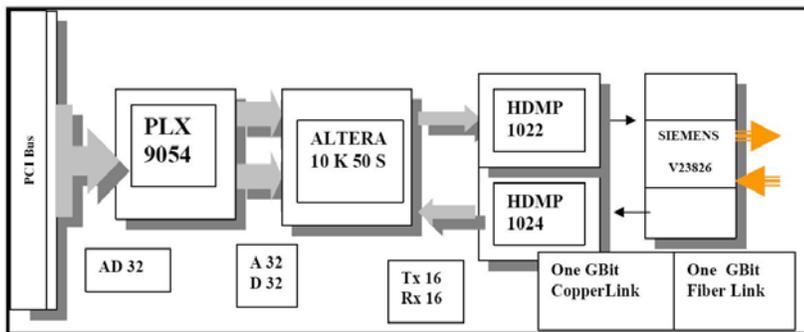


Figure 15-1: IRACE PCI board.

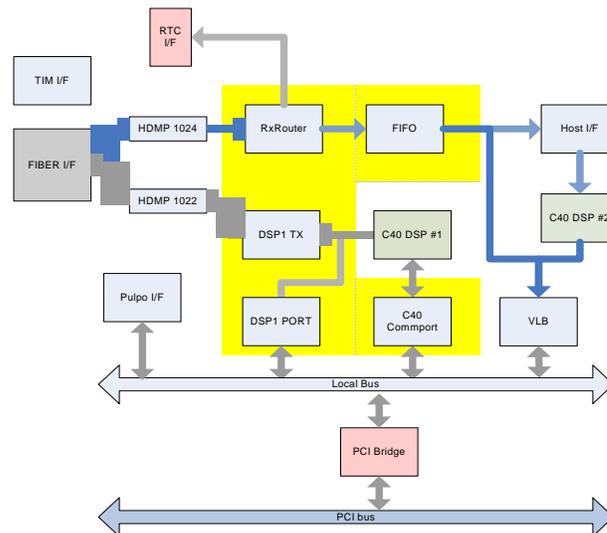


Figure 15-2: FIERA PCI board.

The minimum set of functionalities on this board could be (open to discussion):

- Interface to optical fiber module.
- Real-time command scheduling in writing to the optical fiber module. (Real-time scheduling is needed in order to run seamlessly commands on the front-end.)
- Command response scheduling.
- DMA engine.
- Embedded real-time processing if we decide to implement it as discussed in Section 13.

Apart from the functionalities listed above, FIERA PCI board features additionally a fiber interface to PULPO-II, the interface to TIM (ESO standard Time Interface Module for absolute time event triggering) and the interface to the RTC (Real Time Computer). Because of this, the question here is what other functionalities this board should support. For discussion purposes, a possible block diagram of such a board is shown in Figure 15-3. In this figure the dash line blocks contain optional functionalities to be brought into discussion.

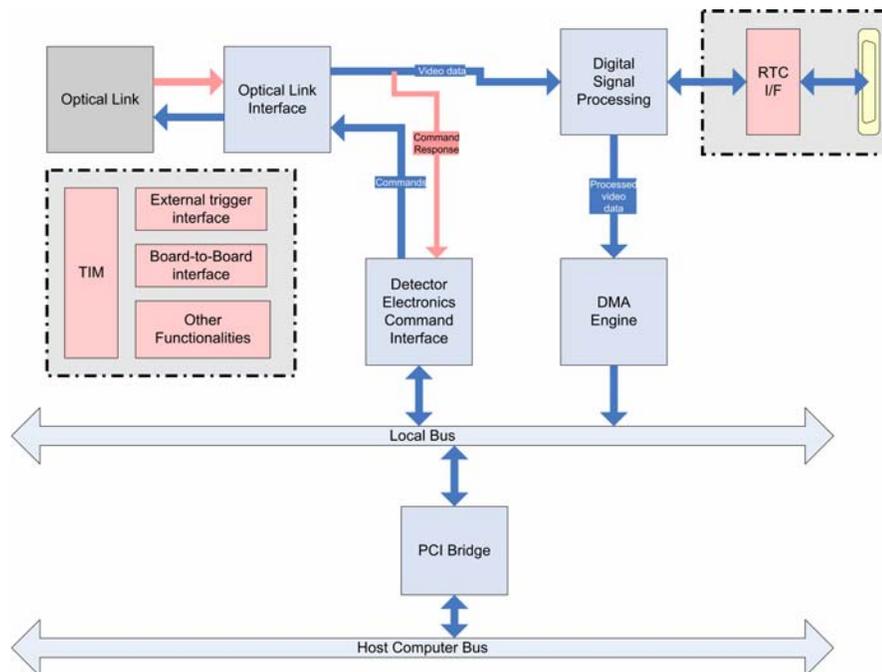


Figure 15-3: Detector Electronics Host Computer board.

The interface board on the back-end computer can be made with a single chip. This chip would contain the bridging from the host computer bus to a local bus, e.g. PCI 32/33, PCI 64/66, along with the interface to the optical transceivers, DMA engine and any additional on-board control logic. However, as the bus of the host computer has changed over time (in the last years has moved from PCI 32/33 to PCI 64/66 and in the forthcoming years PCI-Express might be the chosen bus for computers), a more flexible solution would consist on a two-chip solution for this interface board.



Referring to Figure 15-3, a two-chip solution means a specialized chip for the bridging from the host computer bus to a local bus, e.g. from PLX, and a complex FPGAs for the rest of functionalities, i.e. optical transceivers interface, DMA and additional control logic. By having a two-chip solution, the interface board can be better adapted to any forthcoming new bus. In addition, for the little amount of board that we will produce for the NGC (little amount in comparison to industry production levels) a two-chip solution is more cost effective.

Discussion on the back-end interface board :

- Define set of functionalities covered by this board.
- To easily cover forthcoming buses on the host computer platform: One-chip or two-chip solution?

16 Some Other Functional blocks on FIERA and IRACE

16.1 Analog-to-Digital Converters

Both FIERA and IRACE use 16-bit ADCs. They both started using the ADC from Analogic (ADC4325 at 500kS/s, ADC4320 at 1MS/s or the ADC4322 at 2MS/s for the more demanding applications).

There seems to be no need to move from 16-bit ADC to something like 18-bit ones. However, that does not mean the architecture must foresee only 16-bit buses for the data pixels because if real-time processing is done on-board, the MAC (Multiply-Accumulate) operations can generate more than 16-bit raw pixels data.

Nowadays there is no need to use expensive ADC like the ones from Analogic whose cost is in the order of 1000 euros. IRACE is currently using a very compact and inexpensive ADC from Linear Technology (LTC1608) and the ODT has prototyped and obtained promising results with similarly compact and inexpensive ADC from Analog Devices (AD7671).

16.2 The sequencer

The sequencer both on FIERA and IRACE is a well designed and mature building block which is able to run synchronously and seamlessly a clock pattern with a resolution down to 25ns in FIERA and 50ns in IRACE. Therefore it seems that this part does not need to be redesigned. However, the sequencer should be implemented in a FPGAs from Xilinx (e.g. Virtex-II Pro) as they are currently implemented on Altera FPGAs??? in IRACE and Lattice FPGAs in FIERA.

16.3 Clock voltages

Refer to document: “Next Generation detector Controller: Requirements Specifications”. Doc. Number: XXX-XXX-XXX-XXX.



16.4 Clock waveform shaping

FIERA supports waveform shaping on its clock board in order to optimize CTE and minimize spurious charges when reading CCDs. It is still an unresolved issue the way to reduce spurious charge generation on L3Vision CCDs and for that reason waveform shaping capabilities must be carried over to the NGC.

This feature is implemented with fast static RAM and fast DAC (Digital-to-Analog converters). If this feature is to be maintained on the NGC, the discussion should be centered on whether the current implementation is not exaggerated and an implementation with smaller board footprint would fulfil the requirements.

(There is no need to do clock waveform shaping on infrared devices.)

17 PCB Real Estate statistics

Before any concrete design work, it might be important to measure the amount of space taken by some functional blocks in IRACE and FIERA in order to know before hand the amount of channels that one board can host.

Some data already collected and measured:

- In Monsoon, with a combined clock and bias board and with equal number of number of those, the bias area takes 15% of the board.
- On the video board of FIERA, the clamp-and-sample takes 26% of one analog chain.
- On the video board of FIERA, the digital part takes 35% of the PCB area, the rest is analog.

18 Some areas to be investigated before taking any decision on the final architecture

There are certain areas which could determine the architectural path to follow on the design of the NGC. The specific information on these areas is scarce and should be further investigated before taking a decision. The list may become long but so far these are the areas encountered:

- Serial Switched Fabrics interference to analog signal. If the backplane is to carry the high-speed serial bus signals and the analog signals connected to the detector, the interference between these two groups of signal should be quantified to see if it is a showstopper.
- For CCDs, the performance of digital clamp-and-sample has to be compared to the current analog clamp-and-sample.
- In order to better estimate the maximum number of channels to be hosted in one board, no matter what type of board, more thorough real estate PCB assessment should be done.



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- (Not related with the architecture): switching or linear power supply.