Guard Ring Optimization

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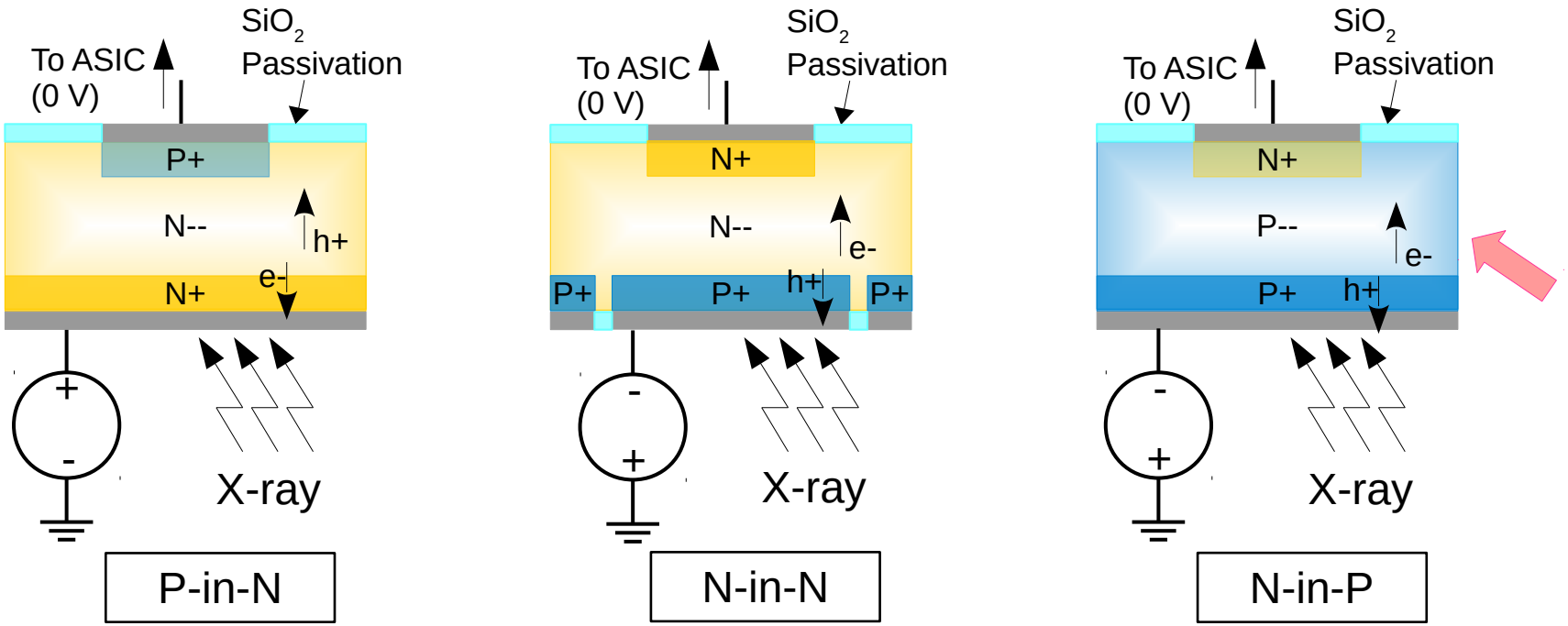
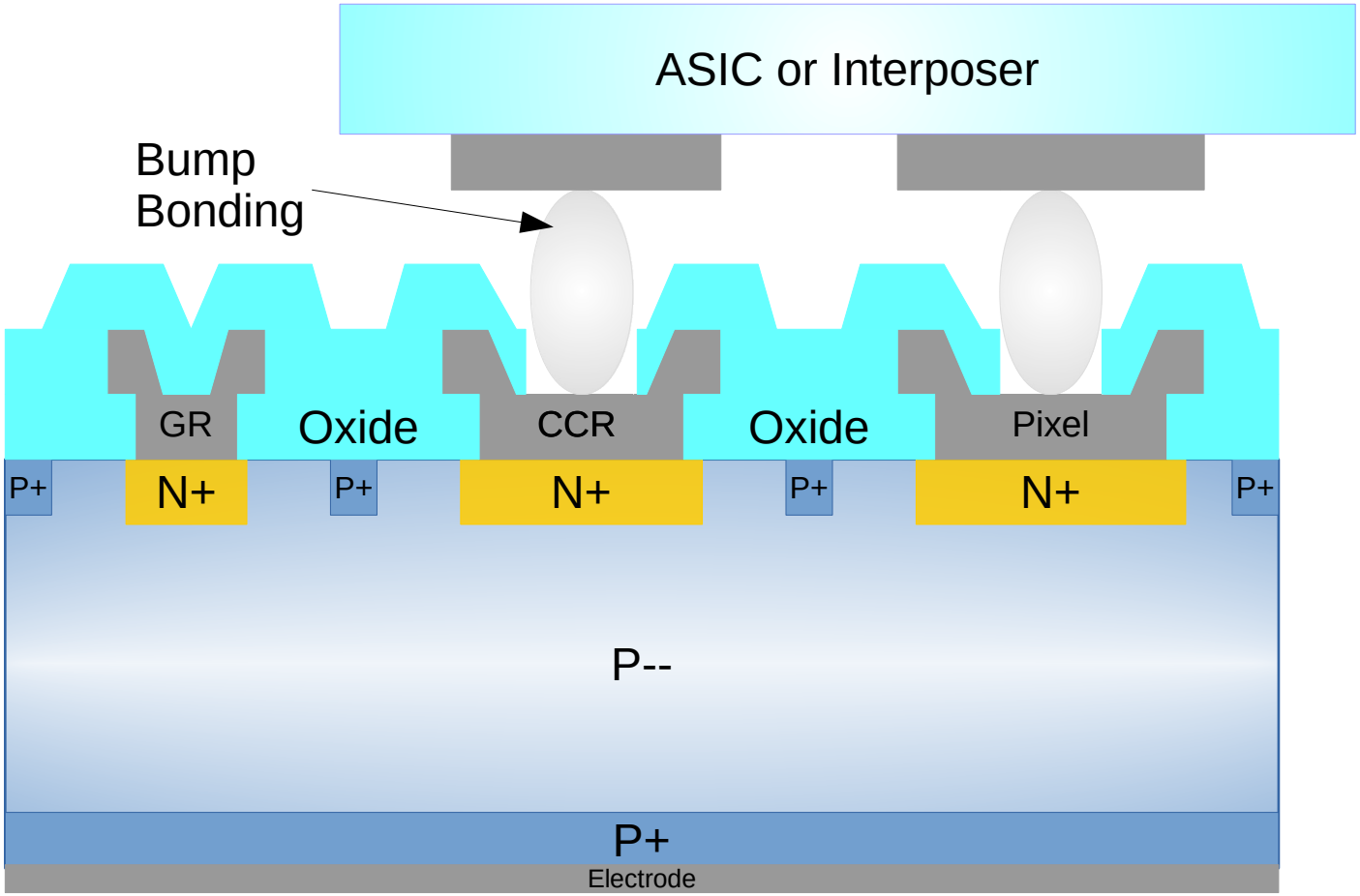
(January 20th 2016)

Silicon Diode Detectors

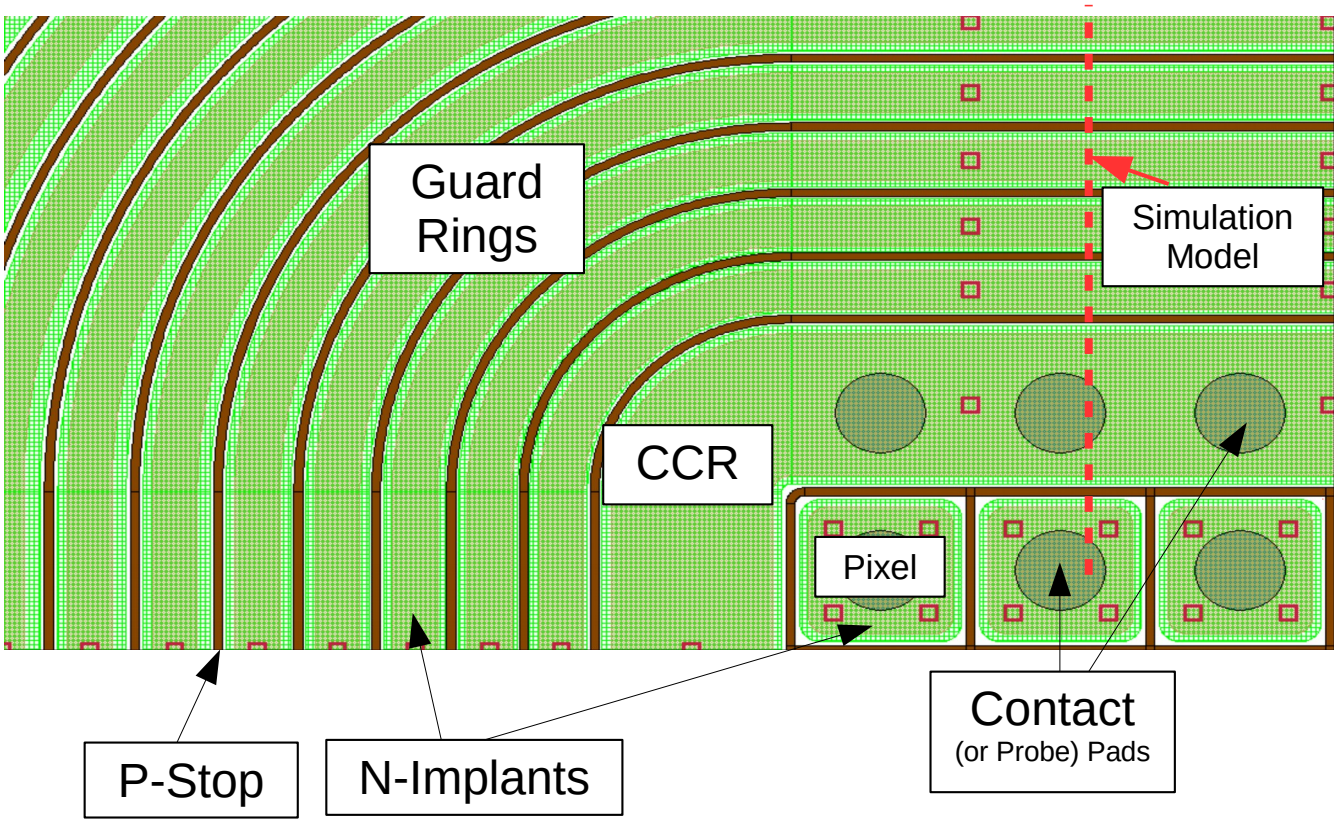


- P-in-N: Most widespread technology so far due to simplicity and affordable substrate from FZ process. However, uses rather slow holes as a main signal carrier and the substrate type changes after lots of high energy X-ray radiation.
- N-in-N: Faster than P-in-N since **electron** is a major signal carrier. But requires double side process to implement guard rings (The depletion region stretches from the back electrode rather than from pixels) but stronger than P-in-N in terms of radiation hardness. → Problem: So complex to manufacture. (note that process difficulty jumps with mask numbers, exponentially.)
- **N-in-P**: Fast. Also much stronger (in terms of radiation hardness) since the substrate is already P-type. The P-type substrate supply was problematic but not anymore.

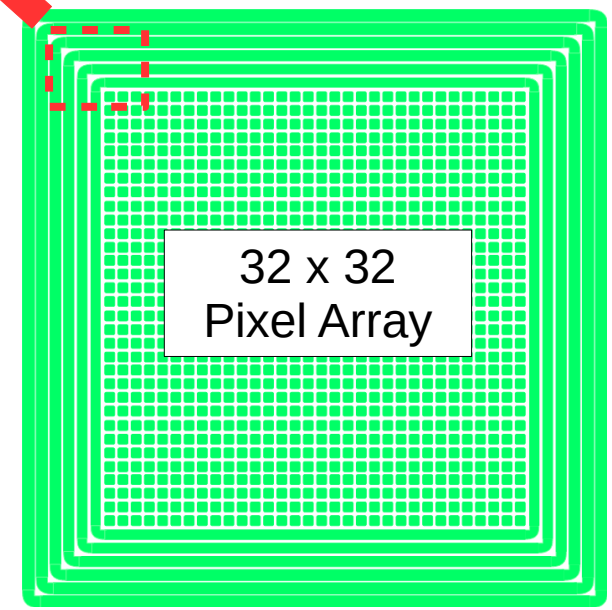
N-in-P Prototype Structure



Mask View of the FASPAX 15 GR Sample

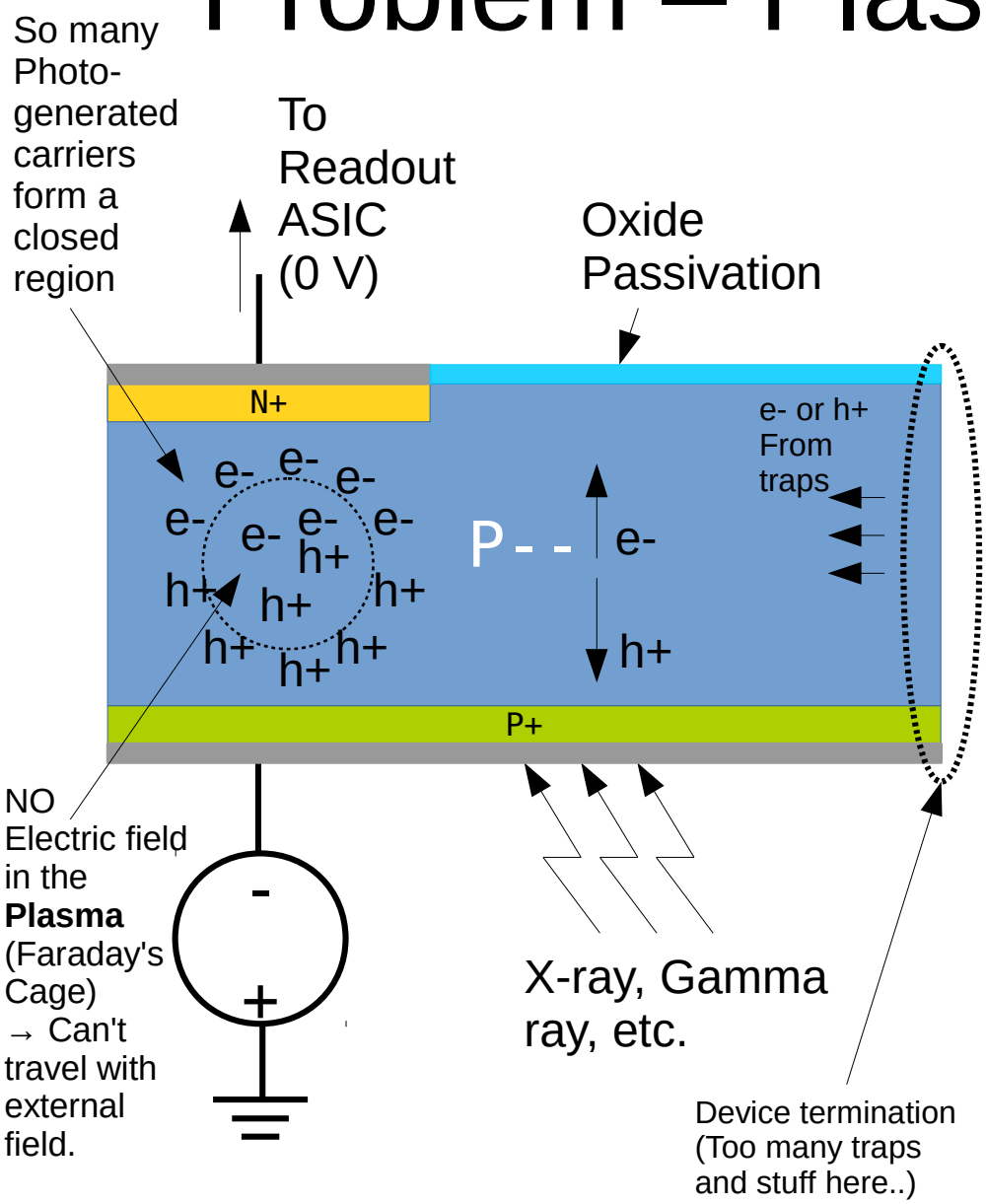


Guard rings are not biased at all.
(Floating Guard Rings)



CCR is a biased (to ground) guard ring which collects additional leakage current.
(Current Collection Ring)

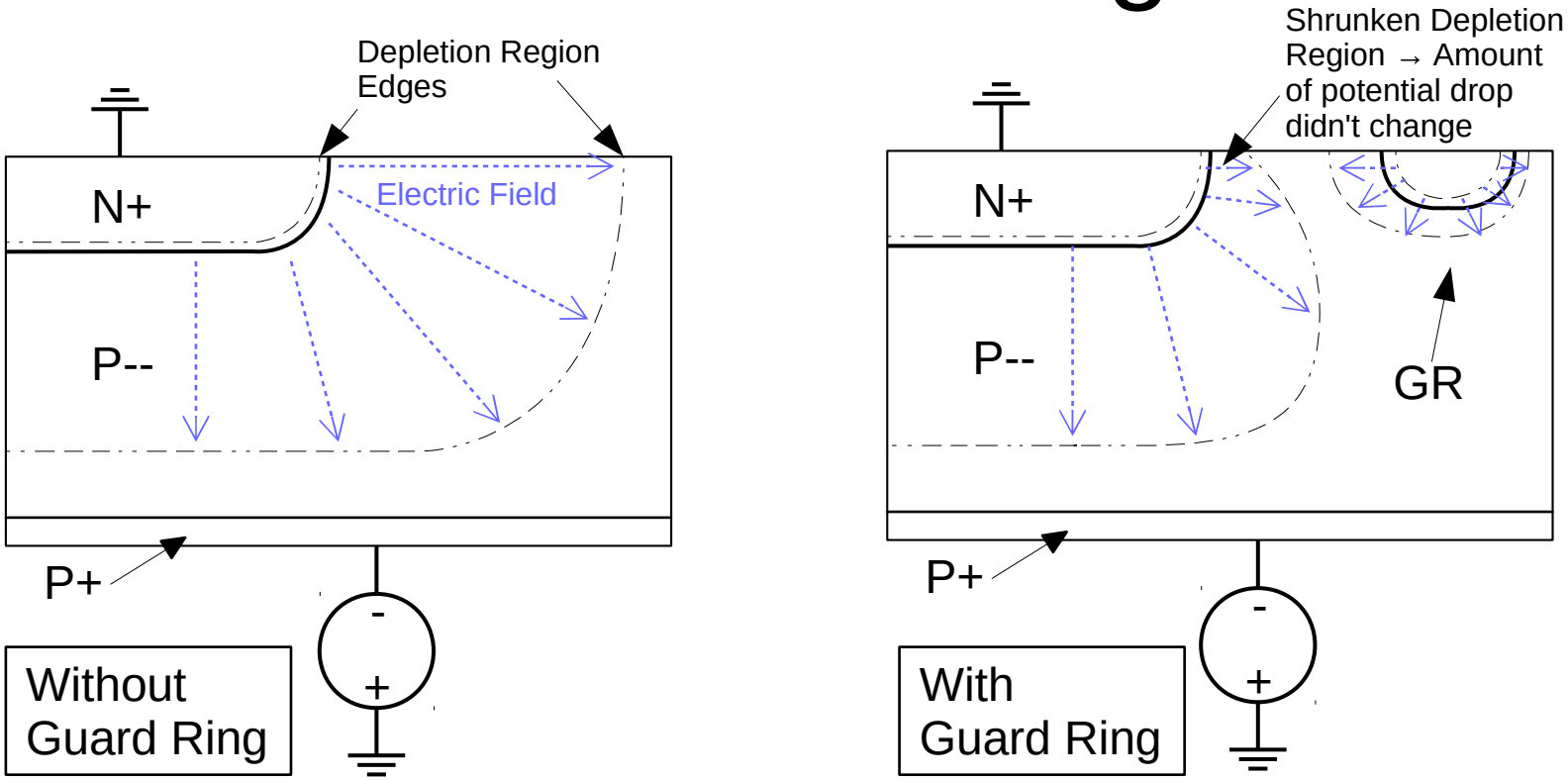
Problem – Plasma Delay Effect



N-in-P Detector

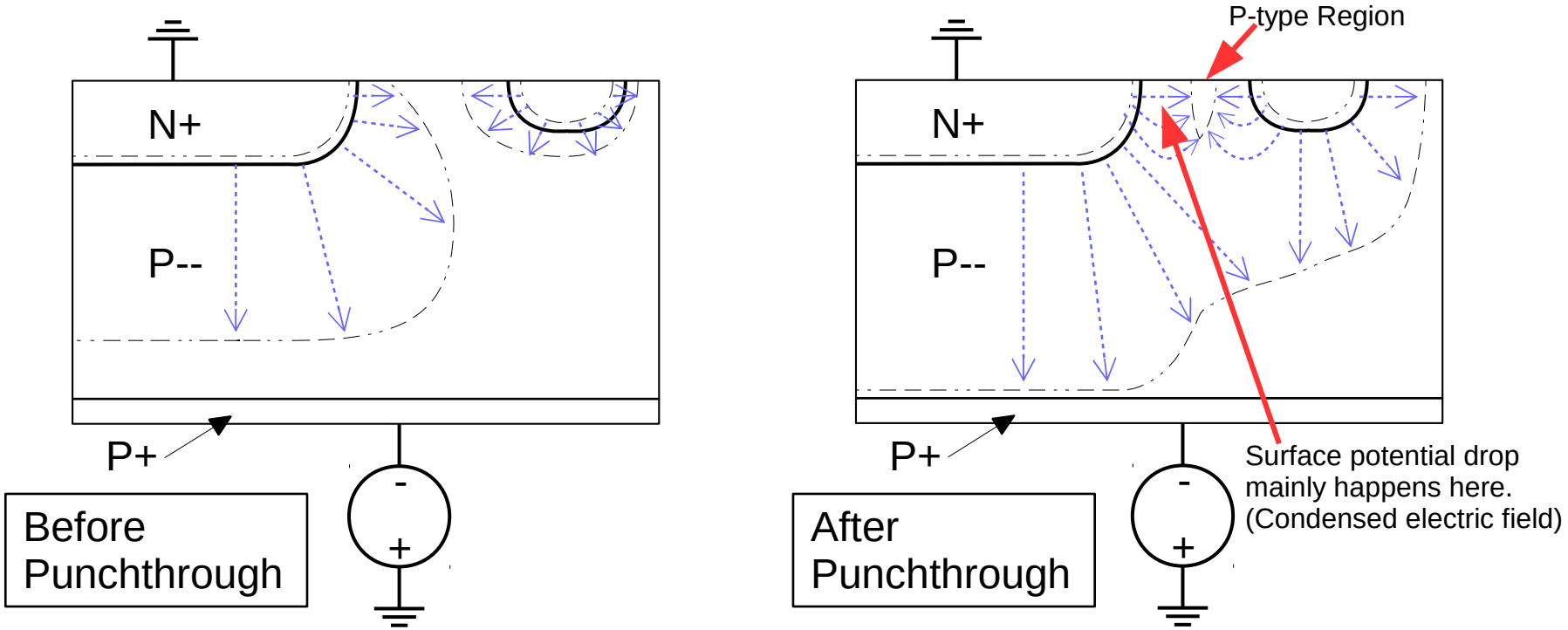
- Problem: the upgraded beamlines emit too many photons per bunch → causing Plasma Delay Effect
- To avoid such unexpected delay, we need to apply extremely high bias (~ 900 V?) across the silicon detector.
- Such high bias causes additional charge injection from device termination. → Additional noise
- Thus, we need to control potential drop at the detector surface (pixel side) in some way. → Guard rings from power electronics.

The Guard Rings



- Manipulates electric field to prevent it reaching the device termination.
  - When P-N was biased, depletion region extends from highly doped side. And the depletion region incorporates electric field. (Depletion region → Electric field.)
- Commonly used in power electronics.
- Currently, FASPAX project employs floating guard rings to simplify ASIC interface.
- The Guard ring (See right figure) disrupts the electric field advancement.

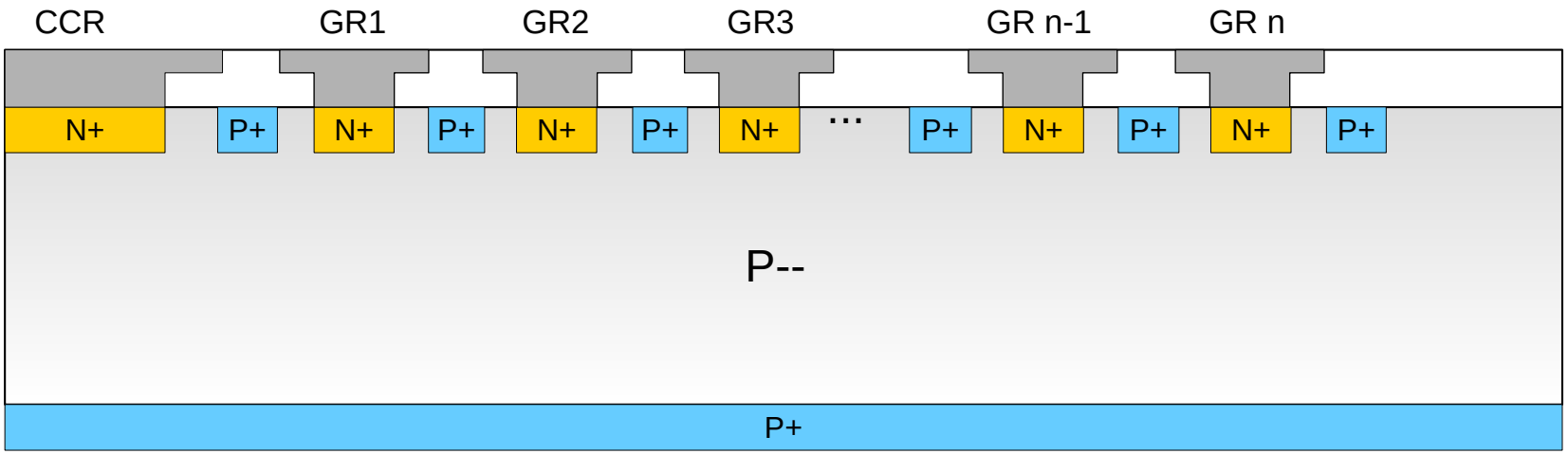
The Punchthrough



- In fact, we need too much bias to avoid the Plasma Delay Effect.
- If the bias is **tooooo high**, a single guard ring is not enough. → The electric field from grounded contact overwhelms GR's counter electric field.
- In this case, we can't rely in N-type guard rings. → So we implemented a small p-type implants before the guard ring to condense the electric field strength even more.

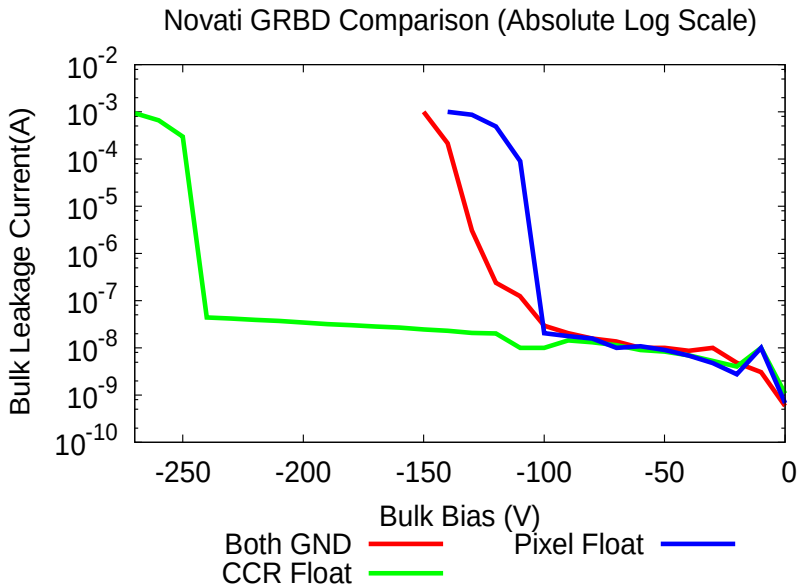
FASPAX Guard Ring Structure

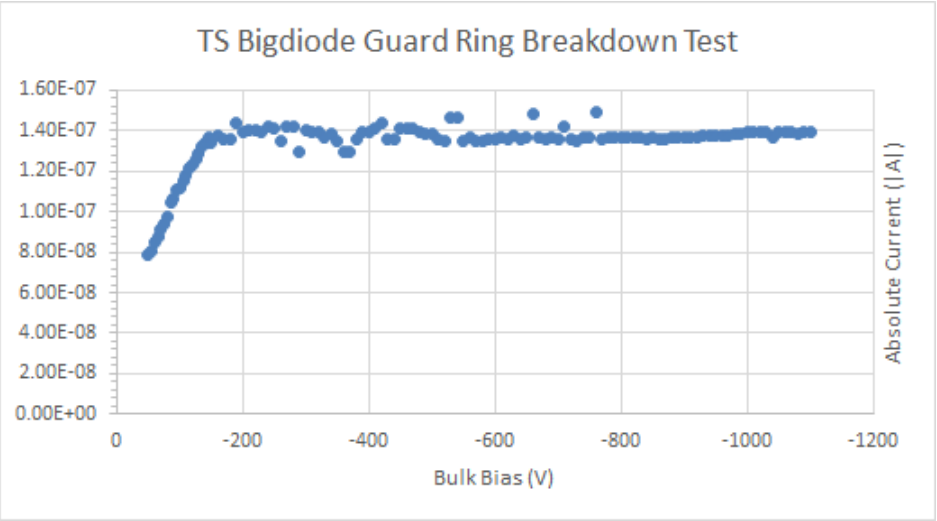
(Simplified)



- Two variants: 8 guard rings or 15.
- Measurement has been performed on test samples has shown that the breakdown (~ -135 V of V bulk.) is actually happening earlier than expectation.
- We suspected the breakdown is actually happening somewhere at the guard ring surface.

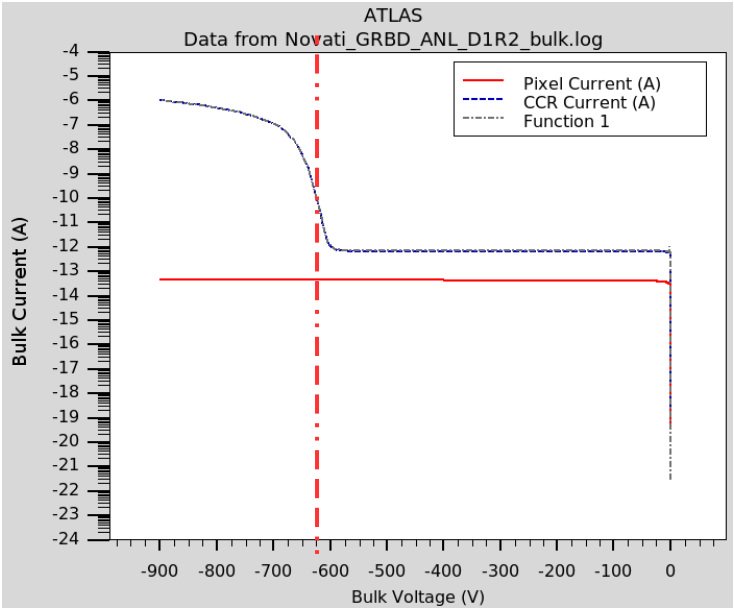
I-V Sweep Results

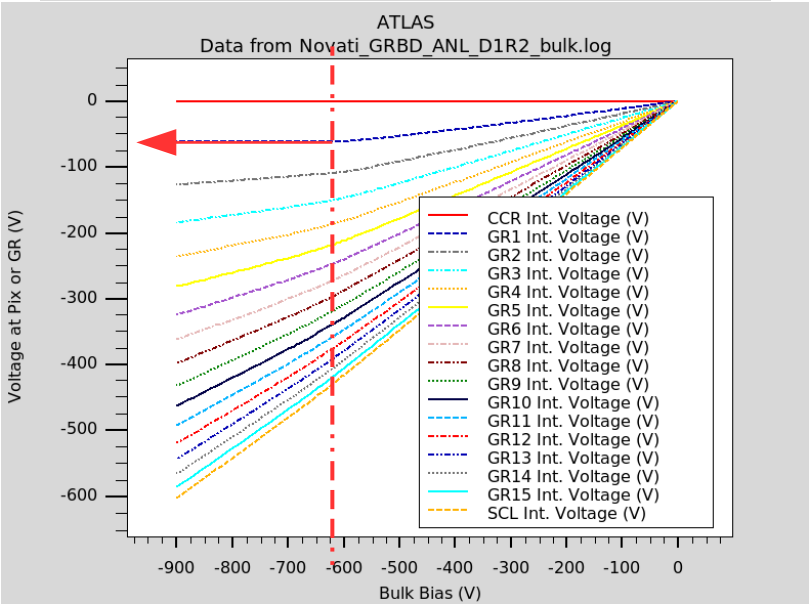




- Upper Figure – FASPAX 15 GR p-stop sample.
  - Breaking down at (as low as) ~ -135 V of bias
  - CCR Float: CCR became a guard ring → improved by twice but not enough.
  - We have taken the data from 16th row pixel.
- Lower Figure – FNAL Big Diode Device with 5 mm-wide, p-stop sample.
  - Two external biased guard ring design. (Similar to Hammamatsu photodiode they were working on.)
  - Also breaking down as low as -200 V.
  - The graph is kind of misleading with the leakage current of 0.1 uA. But, in fact, we had some problem with compliance setting at the characterization system. (One reason why we ordered Keithley 4200.)
  - The voltage bias was actually limited to -185 V due to misleading (1/1000) compliance setting.

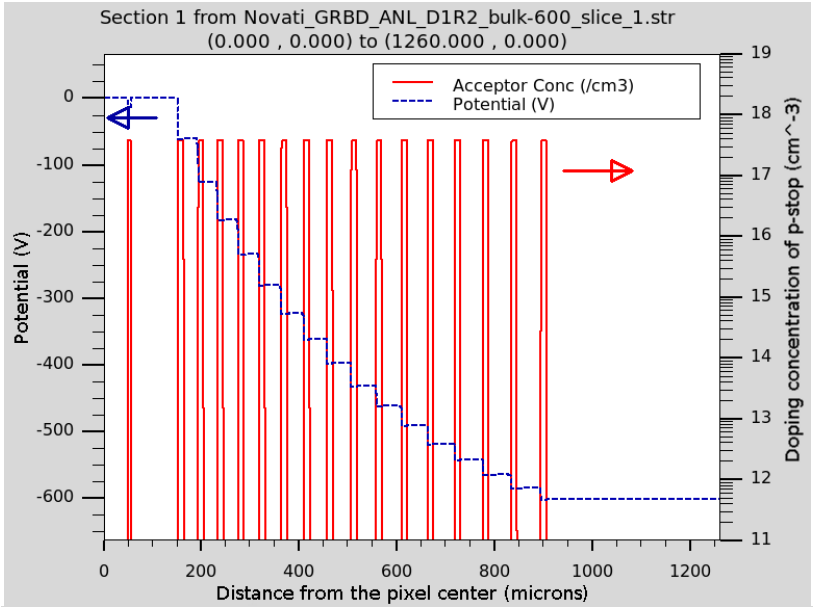
Simulation Result
(I-V, Potential)

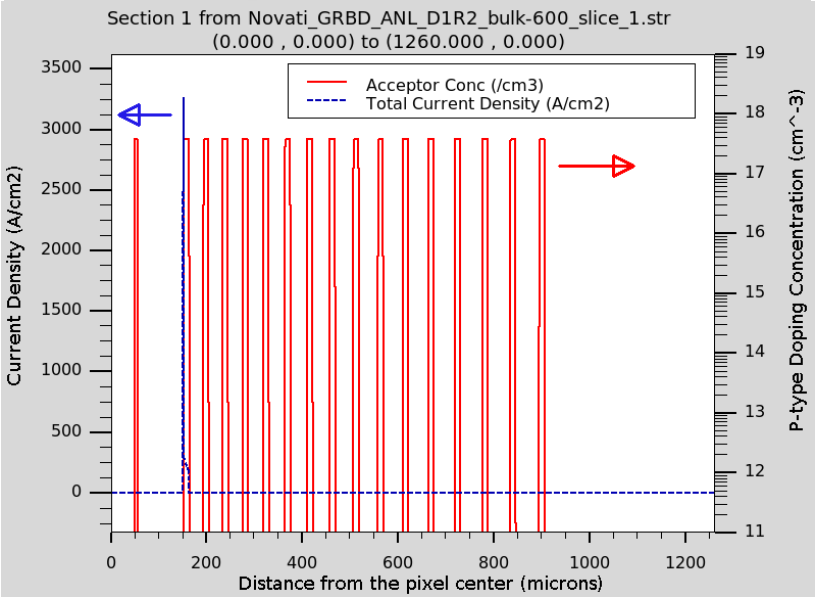




- Breakdown at -630 V.
  - Much higher than expected due to lack of trap state implementation in SiO_2.
  - Also, the bulk silicon was assumed as intrinsic due to numerical issue.
  - This issue was resolved in recent batch of simulation model optimization with higher Q_{ss} of 1e13 /cm^2
- Interface trap (Q_{ss}) was 8.8 x 10^{11} /cm^2. (sheet)
- The Potential of the first guard ring is at -63 V.
- The last floating guard ring potential is staying at -460 V when the bulk bias was -630 (breakdown point.)
  - 170 V bias across the detector at the termination.
  - Depletion region reached here. → Punchthrough control Failed.

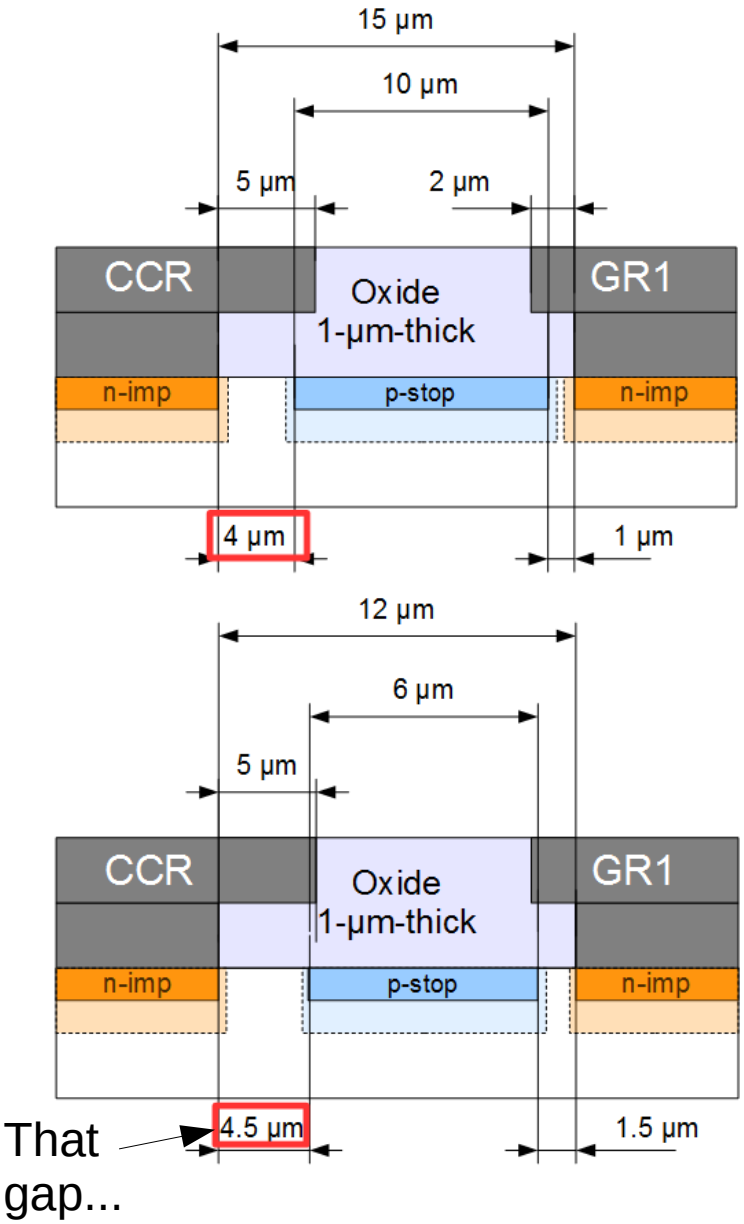
Simulated Breakdown
(Potential, Breakdown Current)





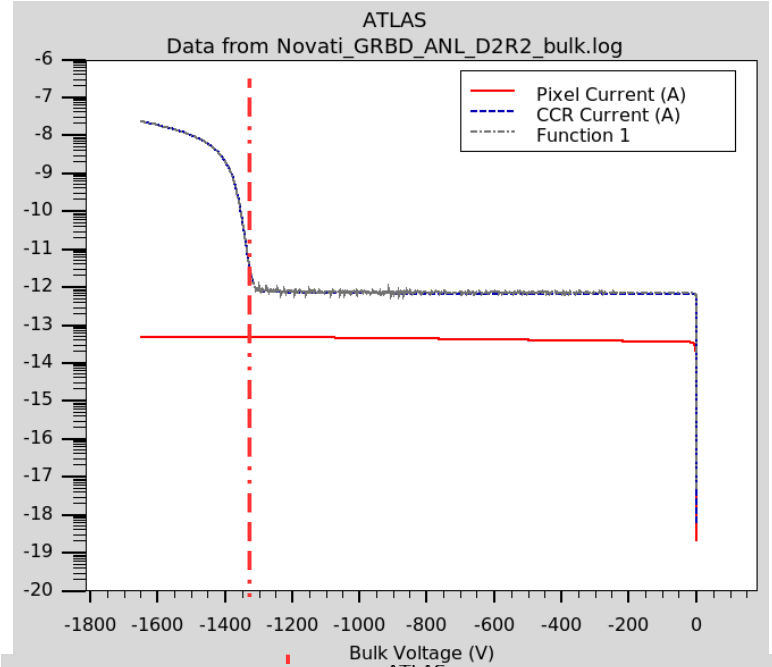
- **Blue line**: Potential and Current density
- **Red line**: Showing the location of p-stop implants.
- The potential drop per each guard ring decreases.
  - Optimal design can be achieved when all the potential drop equalizes.
- Obviously, **the first p-stop implant breaks down**.
  - Its vicinity is actually, N- i-P diode under reverse bias.

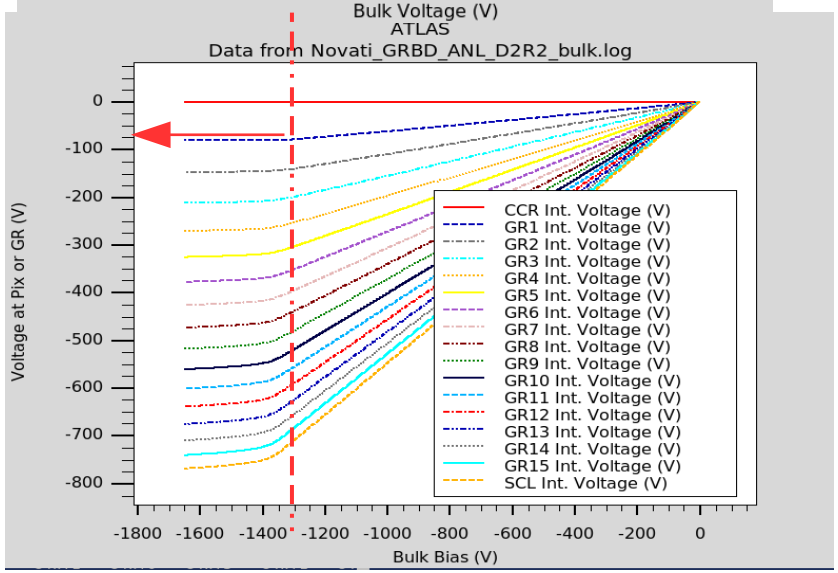
Shorter P-stop Width
(10 → 6 um)



- One way or another, we need to fix the problem.
- Fundamentally, we can reduce doping concentration (either N+ or P-stop) but we don't have direct control on the process.
- Another alternative can be giving more distance from N+ contact to reduce electric field.
- By compromising the design constraints from wafer manufacturer, we reduced the 10-um-wide p-stop implant to 6 um. → Obtained 0.5 um more space.

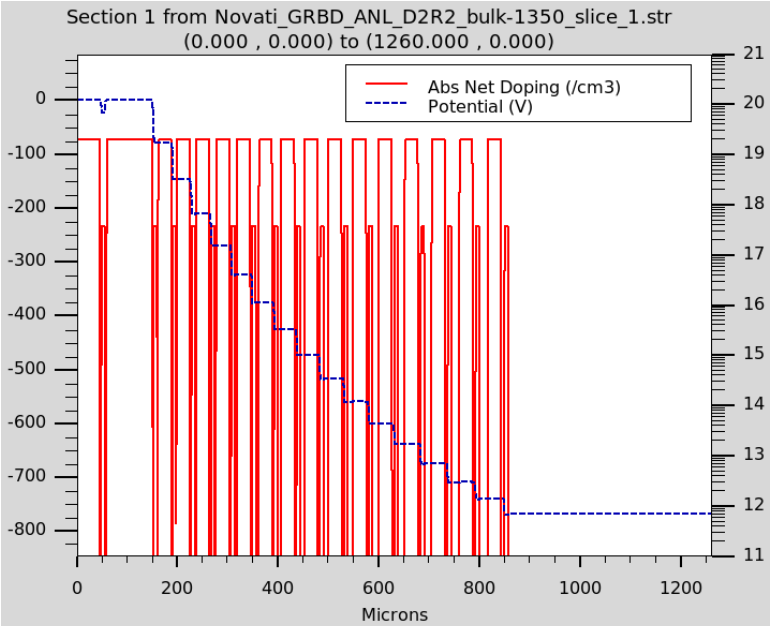
2nd Design
(I-V, Potential)

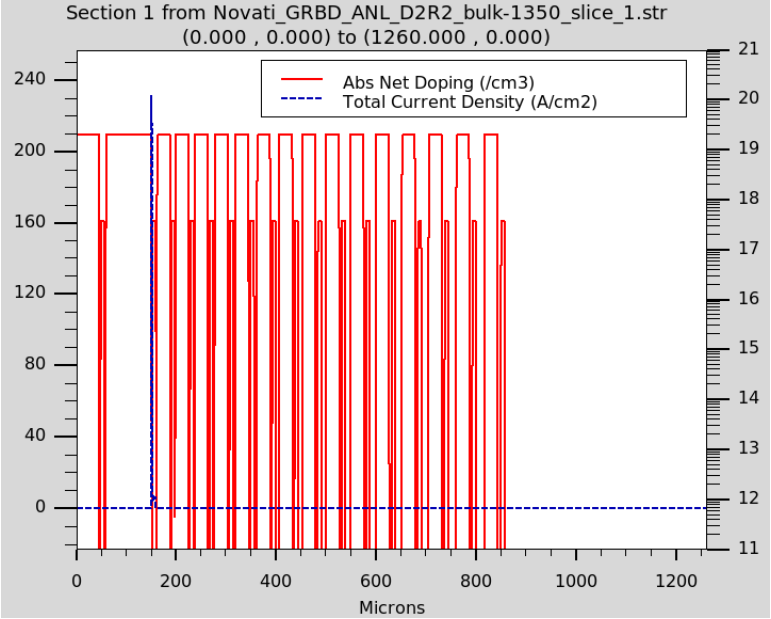




- The breakdown voltage jumped from 10 um-gap design by twice.
- However, still failing at Punchthrough control.
  - Still, the simulation was obtained without proper bulk impurity.

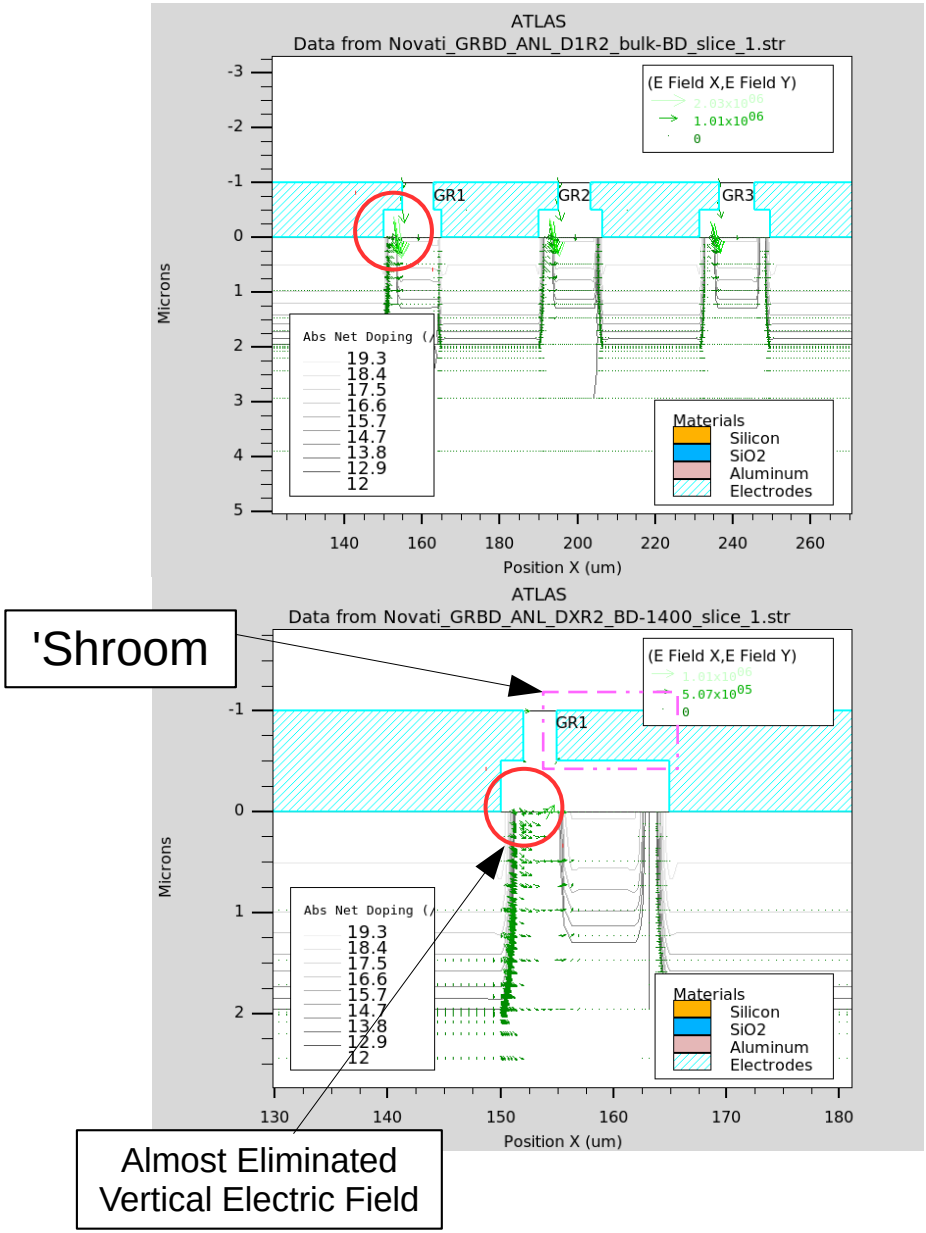
2nd Design
(Potential, Breakdown Current)





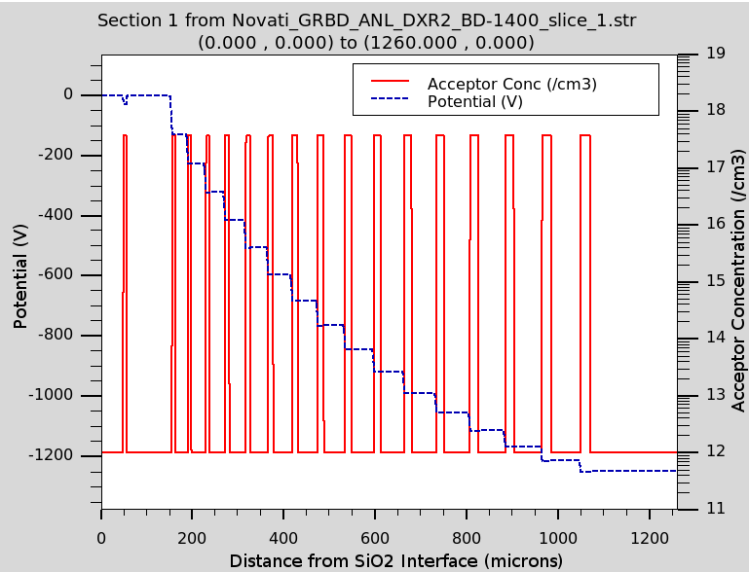
- Potential drop profile seems to be similar to previous 10 um design.
  - We would rather need to ***spread*** the GR implants.
- Again, the breakdown actually happened at the first guard ring.

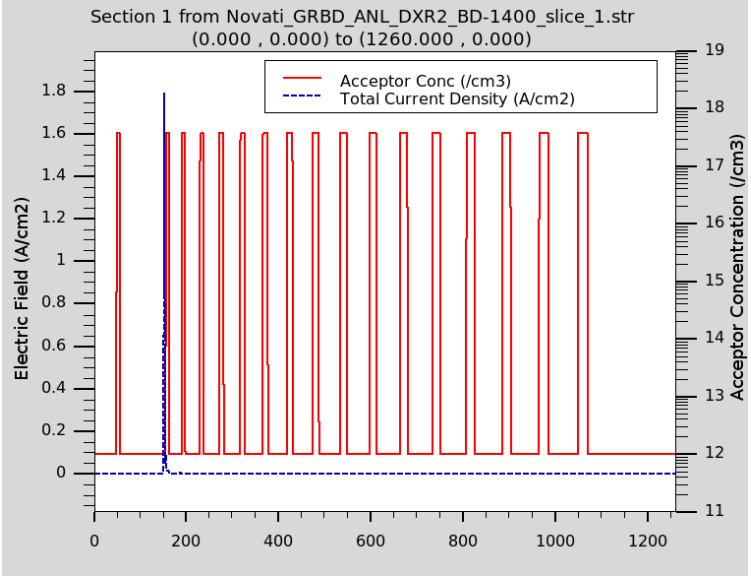
3rd Design ('Shroom?)



- Sounds weird, but the overhang from previous (or left) electrode overlapping p-stop causes tons of electric field.
- Mainly, it is vertical direction and doesn't seem to be significant to the reverse biased N-i-P vicinity.
- However, O. Koybasi, et al. pointed out that the vertical electric field can be a menace.
- So, we decided to move the p-stop towards to next n+ implant and extended guard ring overhang → ('Shroom)
  - In fact, they point out that the 'Shroom doesn't need to be too long. So we stayed at 9 um-long to just cover the entire 6 um-wide p-stop implant.

3rd Design
(Potential, Breakdown Current)

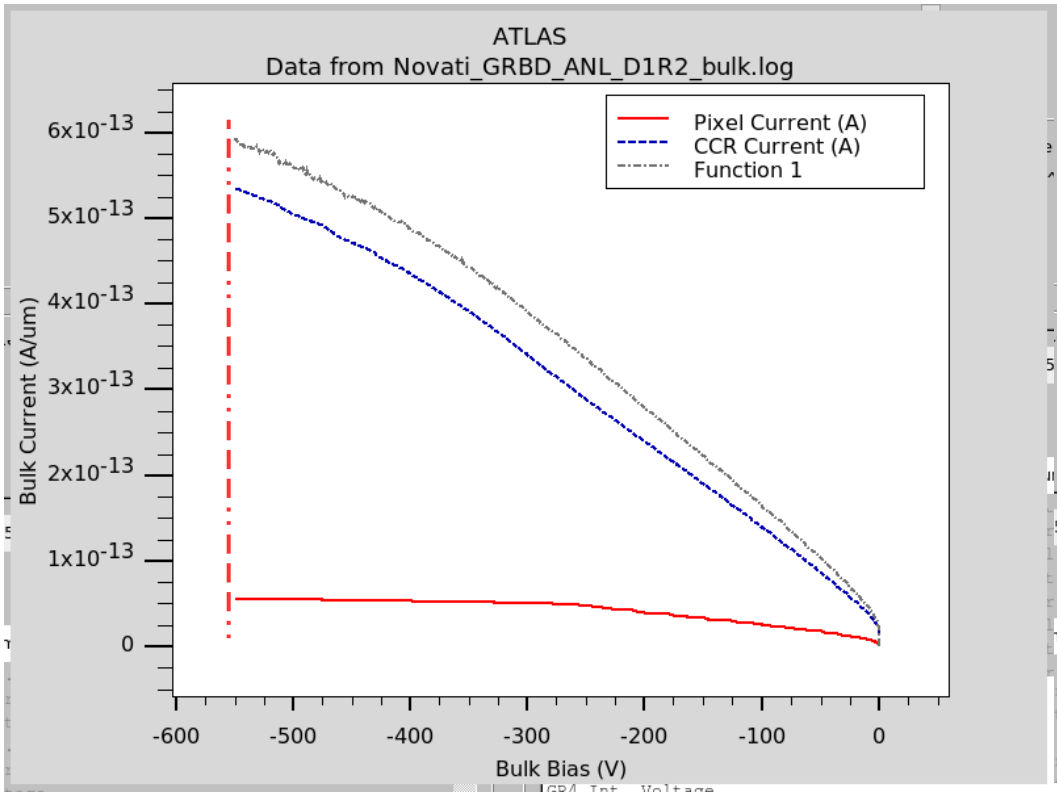


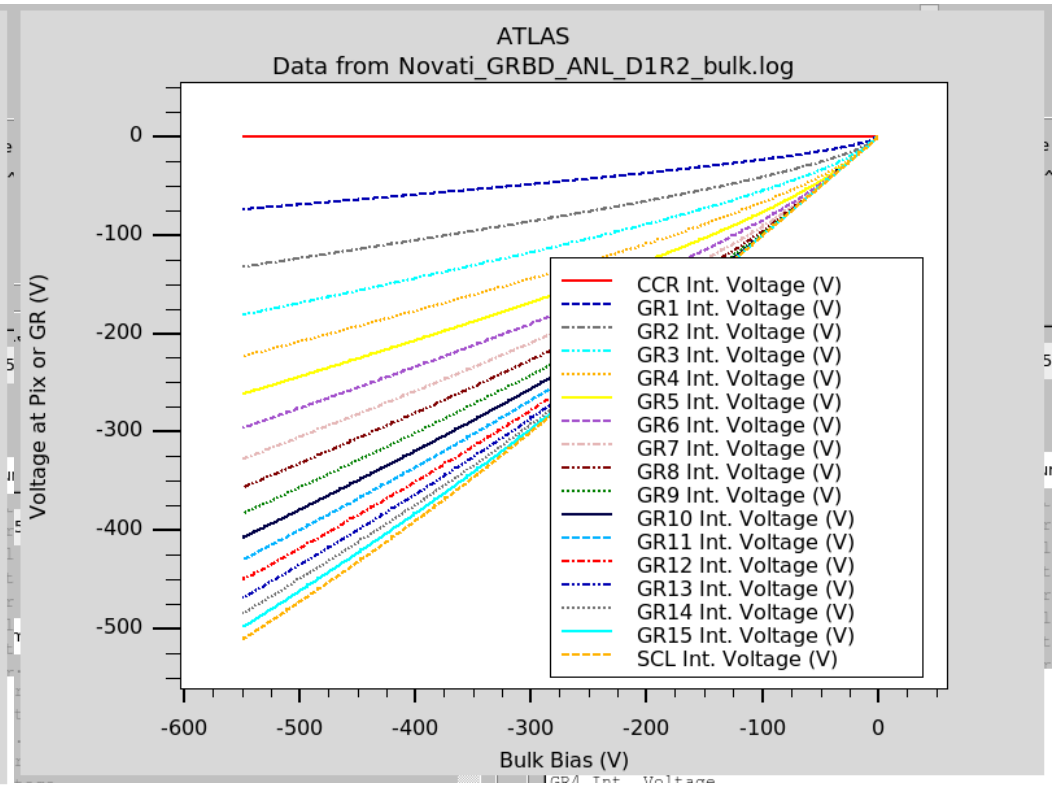


- Again, It breaks down at the first guard ring.
- The first guard ring sustains up to -120 V of bias which is technically doubled from previous design.
- The breakdown actually happened at -1250 V of bulk bias. → This time, the bulk is not intrinsic!! 1e12 cm^-3 of Boron
  - Such bulk implementati
    prev. device breakdown
    -750 V...
- Also, the last guard rin
  is as low as -1250 V →
  controlled the Punch
- So, **I guess we nailed it!!**

Comparison of three devices with proper bulk impurity of 1e12 /cm^3

1st Device with Bulk Impurity (1e12 cm^-3 Boron)

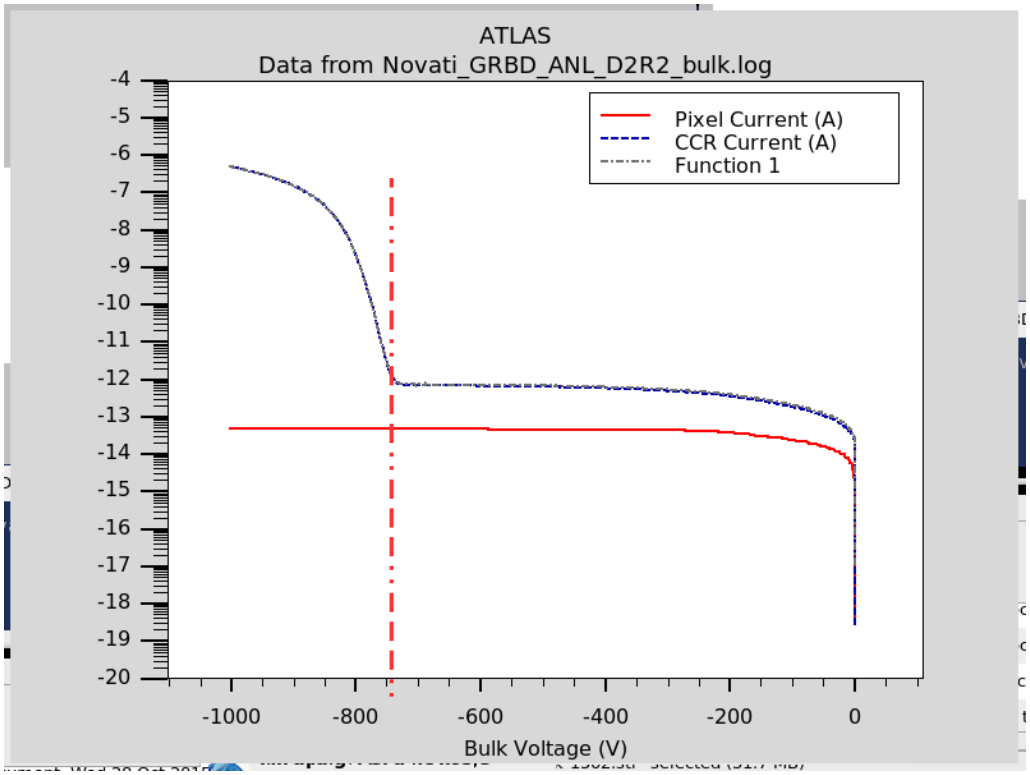


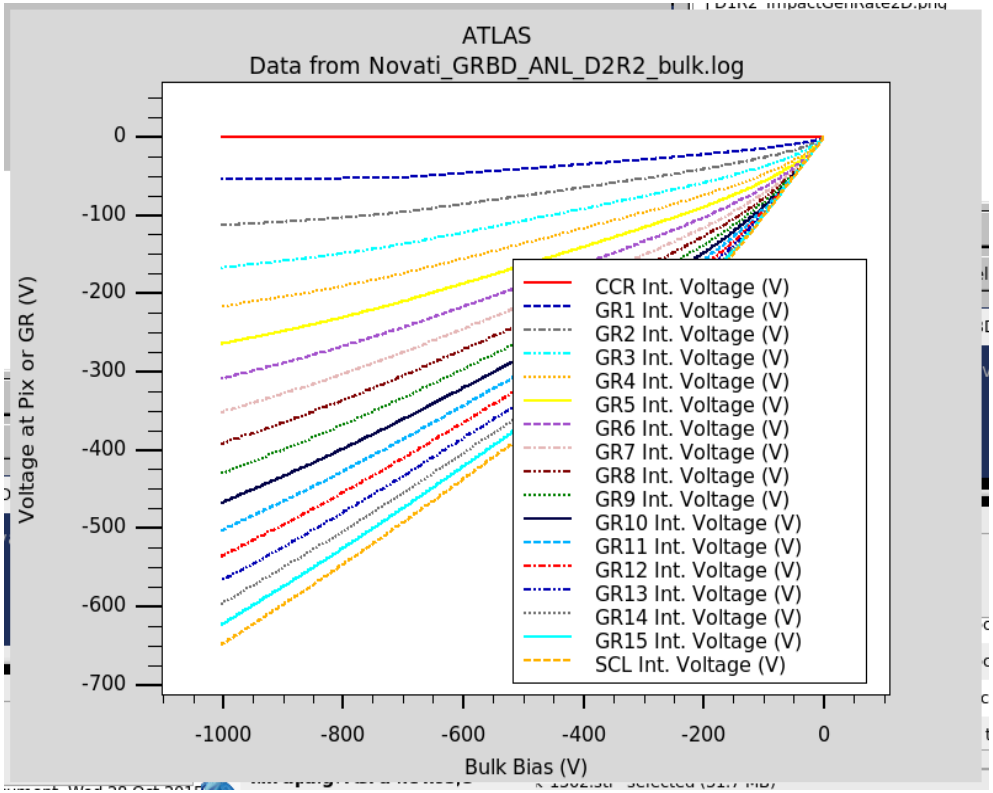


10-um-wide p-stop device:

Breakdown at -560 V? → Simulation convergence issue
Potential at the last GR: -510V → Punchthrough

2nd Device with Bulk Impurity (1e12 cm^-3 Boron)

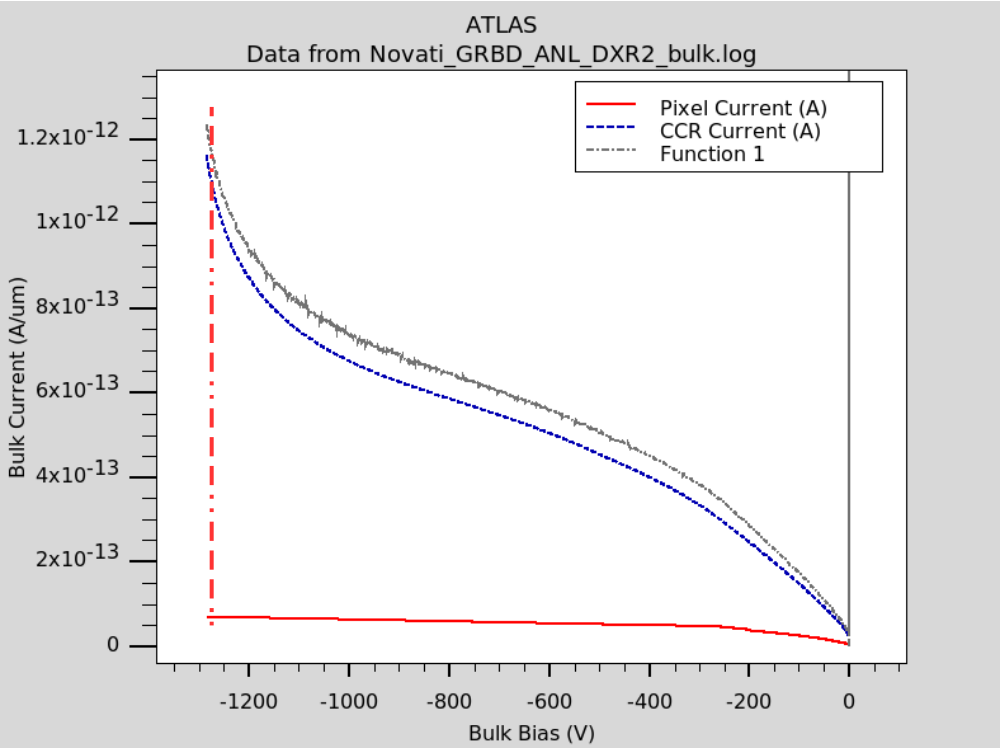


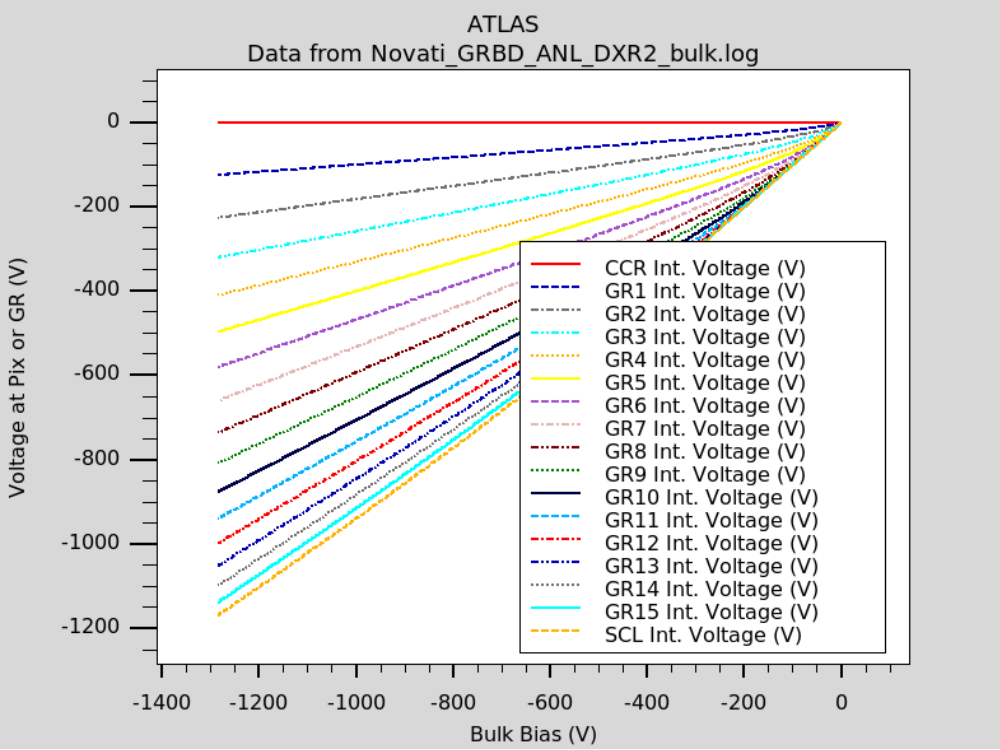


6 um-wide p-stop device.

Breakdown at -750 V
Potential at the last GR: -550V → Punchthrough

I-V Characteristic and potential from the 3rd device





'Shroom device

Breakdown at -1250 V
Potential at the last GR: -1250V → **NO** Punchthrough

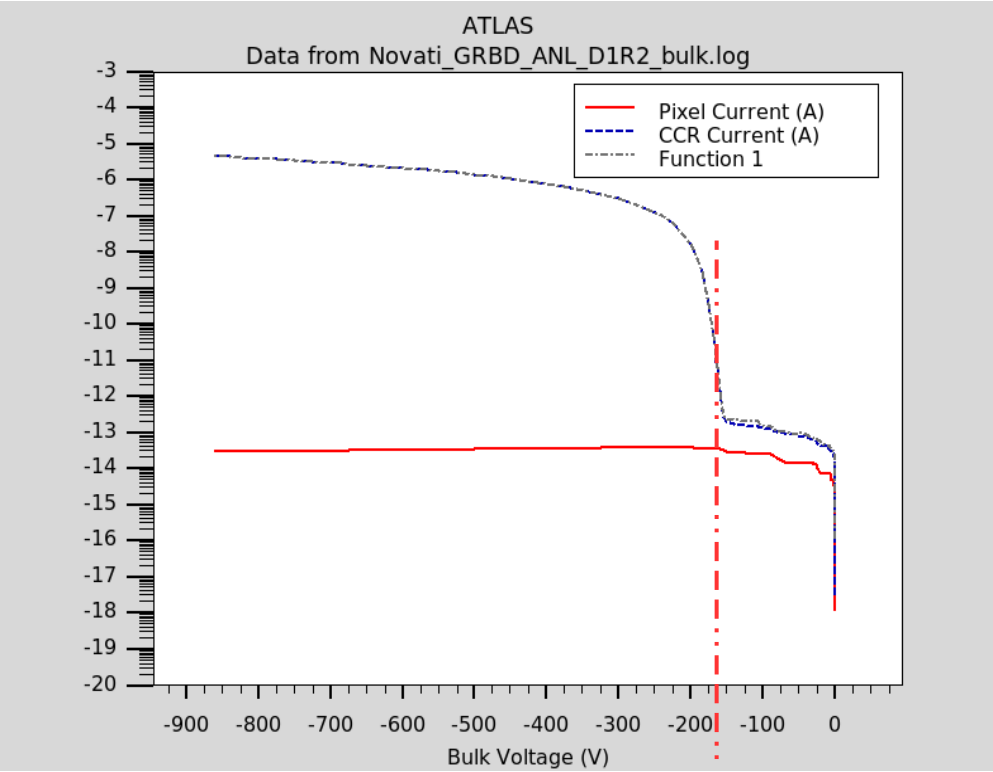
Comparison Summary

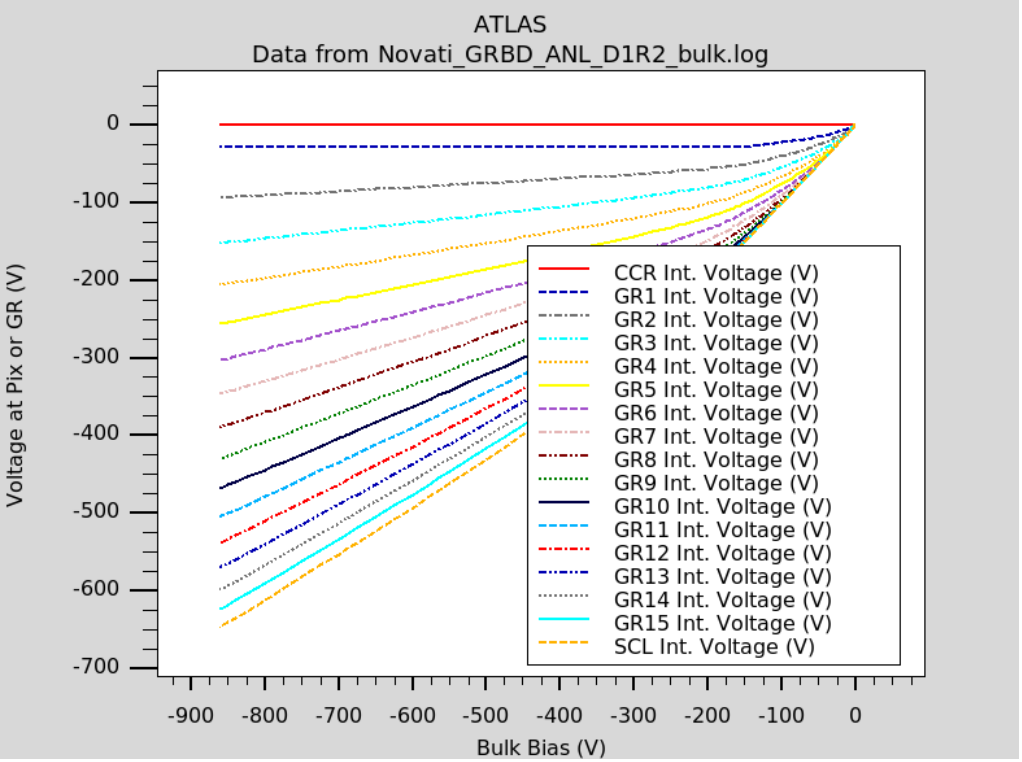
Device Type	Breakdown Voltage	Punchthrough
10-um-wide P-stop	-560 V	No
6-um-wide P-stop (shrunken device)	-750 V	No
'Shroom device	-1250 V	*Yes*

Conclusions

- Unexpectedly, suppressing vertical electrical field resulted a substantial improvement.
  - Not to mention that the distance from N-implant was extended when we moved p-stop implant: pushed down the breakdown point even further.
- However, we need to actually implement and verify the 'Shroom' design.
- According to Nov. 30th meeting, Novati will reduce p-stop doping concentration which would improve breakdown strength even further.

1st Device with Qss = 6.7e12

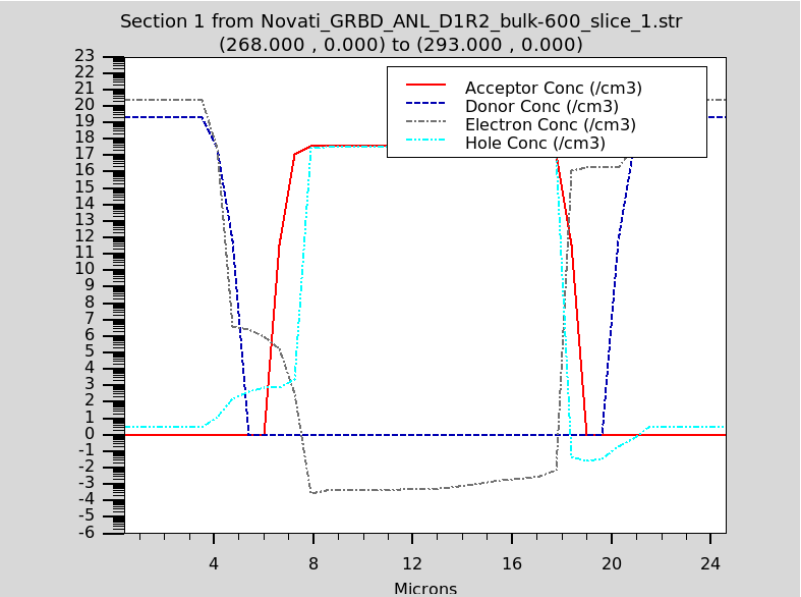


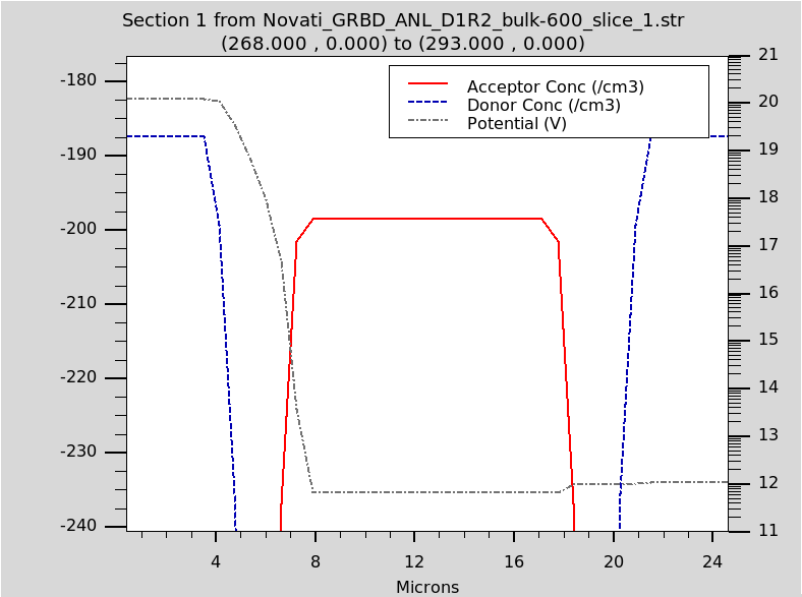


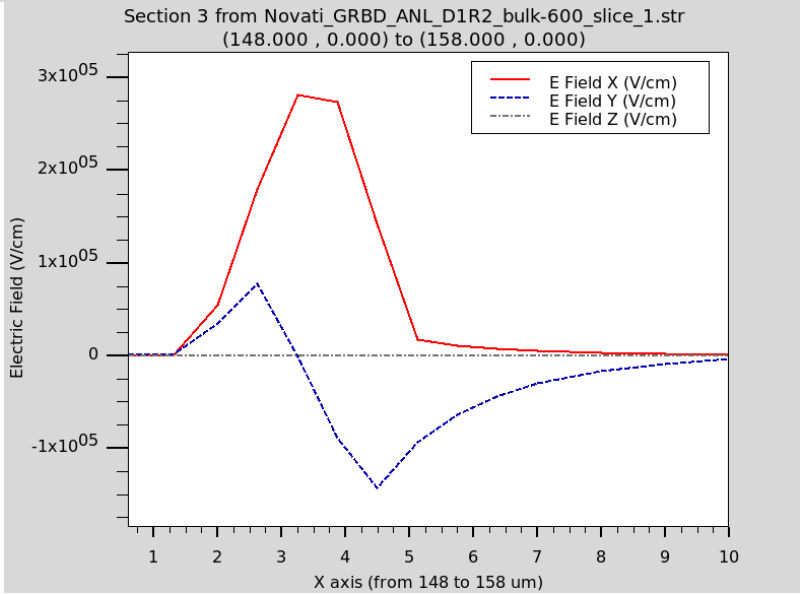
10 um-wide p-stop device with Qss = 6.7e12
→ Such high Qss is normally found in polysilicon TFT process. (where, oxide is 'deposited')

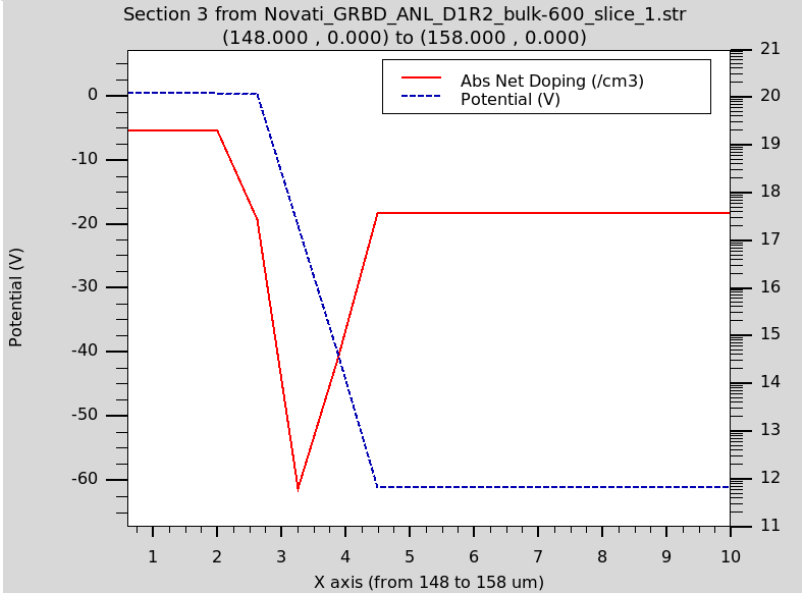
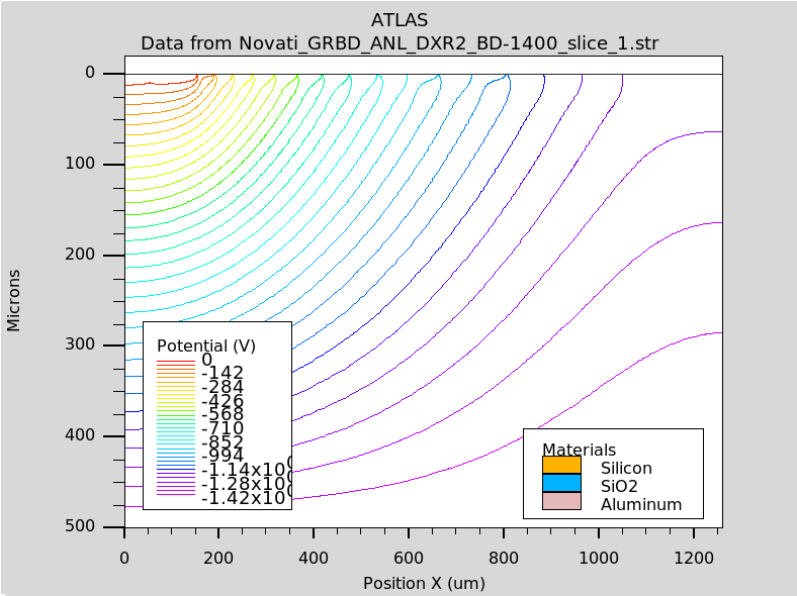
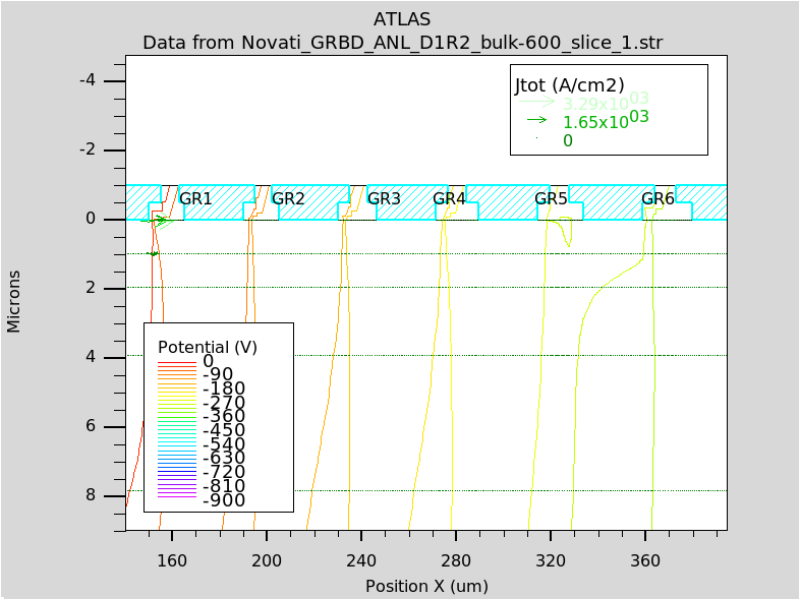
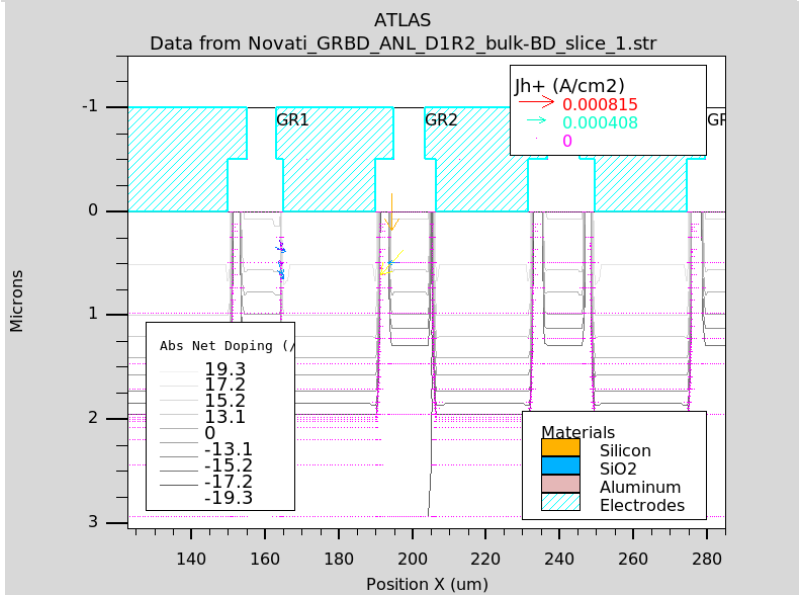
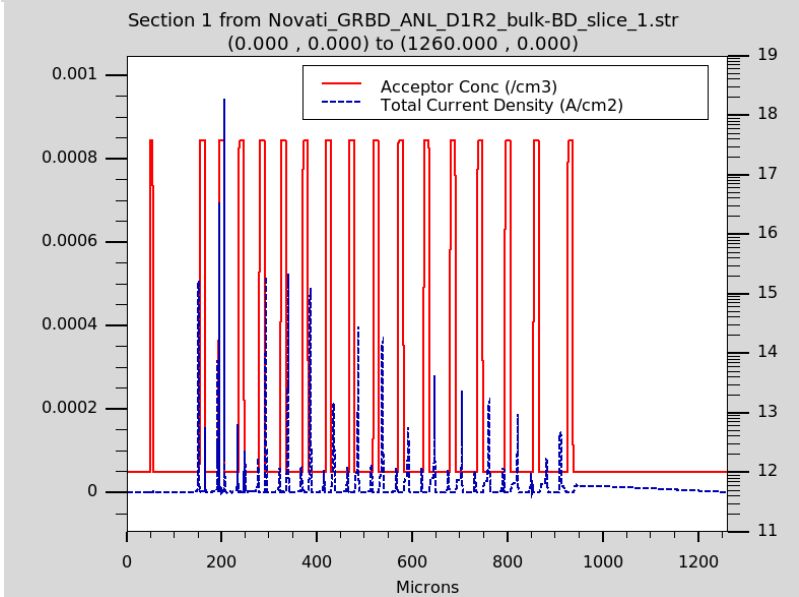
Breakdown at -150 V
→ Punchthrough was not found but the device is useless to prevent plasma delay effect.

E-field and potential at the 1st GR vicinity









Some more fancy 2D contours