

Study of Breakdown Effects in Silicon Multiguard Structures

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Abstract—The purpose of this work is to study layout solutions aimed at increasing the breakdown voltage in silicon micro-strip detectors.

Several structures with multiple floating guards in different configurations have been designed and produced on high-resistivity silicon wafers. The main electrical characteristics of these devices have been measured before and after irradiation. Both radiation-induced surface and bulk damage effects were considered as well. The highest breakdown voltage was found on devices featuring p^+ guards without field plates. A simulation study has been carried out on simplified structures to evaluate the distribution of the breakdown field as a function of the guard layout. The aim was the design optimization.

Index Terms—Avalanche breakdown, full depletion, guard ring, layout, punch-through, semiconductor junctions, silicon radiation detectors.

I. INTRODUCTION

HIGH voltage is often necessary to reverse bias a p^+n junction in many applications to silicon detectors. This is true in several cases: when drift detectors are used, high reverse bias can be applied to ensure a good voltage distribution across the strips. Detectors on very thick substrates require high depletion voltage despite the low doping concentration; high depletion voltages are also needed for detectors exposed to high levels of radiation which cause displacement damage in the silicon lattice and type inversion, with a corresponding increase of the full depletion voltage. The effect is related to the generation of trap levels in the silicon bandgap which affect macroscopic quantities like the full depletion voltage and the junction leakage current. At Large Hadron Collider (LHC)

(CERN, Switzerland), the radiation is mainly due to neutrons and charged hadrons which lose energy via nonionizing processes. Silicon detectors for LHC experiments should be designed to withstand fluences up to several 10^{14} part \cdot cm $^{-2}$, integrated over several years of operation.

Multiguard structures are one of the possible solutions to limit the electric field intensity at p^+n junctions. They consist of a series of concentric floating guard rings which can be biased via punch-through conduction to the central diode [1]. In this way they produce a distribution of the applied potential across a large distance from the main junction. Otherwise, the electron accumulation layer at the Si-SiO $_2$ interface would produce a narrowing of the junction depletion region and consequently higher electric fields. High breakdown voltages can thus be obtained by optimizing the distance between floating guards, which in turn depends on the operational conditions, such as bias voltage and radiation effects.

Many contributions to the study of these structures can be found in the technical literature together with analytical works aimed at optimizing the layout of the floating guard rings [2], [3] and at calculating the breakdown voltage [4]. These studies were developed over ten years ago and they were mainly committed to the power device technology. When multiguards are applied to silicon detectors [5], [6], changes in process parameters like substrate resistivity, implant depth and shape, passivation layer material, and thickness must be taken into account and the optimization procedure needs to be reconsidered. In addition, structures presenting a large number of guards increase enormously the complexity of an analytical approach. Finally, the irradiation induces modifications of the electrical behavior of these devices. Ionizing particles create positive charge, eventually trapped into the oxide with a resulting strong surface accumulation and narrowing of the depletion region width [7]. On the other hand, hadrons produce changes in the effective doping concentration with modifications of the full depletion voltage and of the space charge region (SCR) extension [8].

In previous work, we examined multiguard structures having different layouts and simulated their behavior with encouraging results [9]. Nevertheless, those devices did not allow for a complete comparison between different solutions and they presented some problems after heavy radiation damage, (i.e., at fluences $\sim 10^{15}$ cm $^{-2}$).

New sets of devices have thus been designed and produced. The results of the dc characterization is shown in Section II. In

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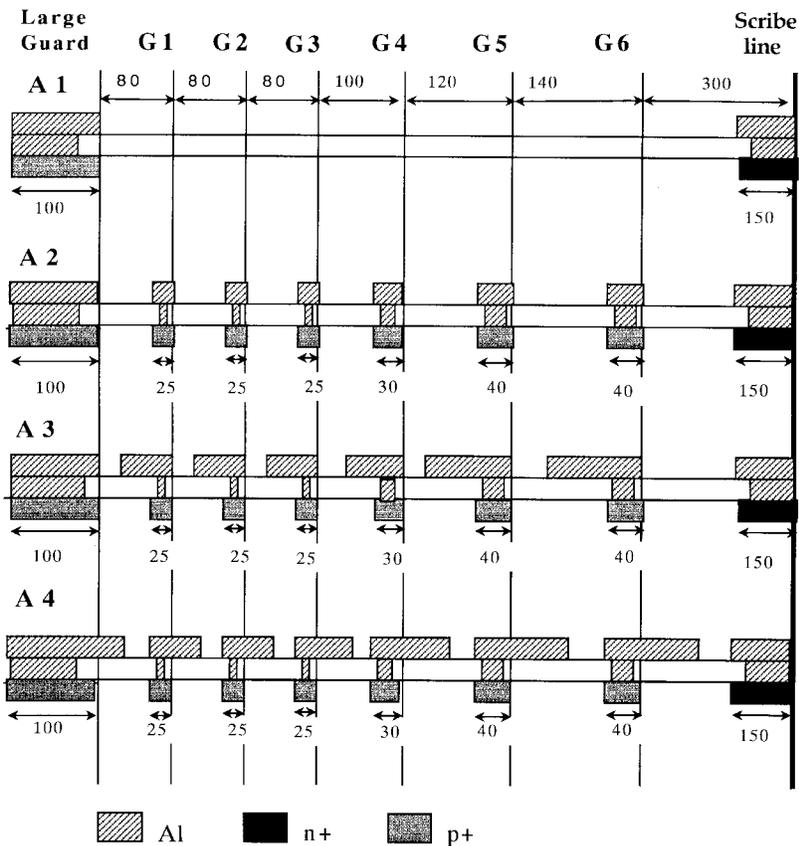


Fig. 1. Set A of multiguards. The large guard is on the left, while the scribe line through the n-well is on the right (distances are expressed in micrometers).

the same section, the problem of the distance of the implants to the device edges, particularly crucial after type inversion, is investigated by means of simple structures. Furthermore, the results after irradiation with both γ and hadrons are discussed. In Section III, a simulation work on structures with a reduced number of guard rings is presented. Its aim is to understand which are the important design constraints to be considered for an optimized design, taking into account the radiation effects.

II. EXPERIMENTAL

A. Structure Description

Multiguard structures were designed around both diodes and baby detectors produced by CSEM (Neuchatel, Switzerland) and SGS-Thomson Microelectronics (Catania, Italy) on lightly doped n-type, $\langle 111 \rangle$, and 300- μm (CSEM) and 400- μm (ST) thick silicon wafers. The diodes are $1.5 \times 1.5 \text{ mm}^2$ p^+ square implants surrounded by a conventional 100- μm wide guard (large guard) and by external multiguard structures, extending 900 μm from the large guard edge. Baby detectors feature an area of $8.4 \times 30 \text{ mm}^2$ segmented into 128 p^+ AC-coupled, polyresistor biased strips. The detector area is surrounded by the large guard (which is also the bias line), which is again surrounded by the multiguard structure. Diodes are available in eight different layouts, grouped into two families (set A and B of Figs. 1 and 2). Set A consists of a basic structure with six p^+ guards (A2); field plates have been added, either inwards (A3) or outwards (A4). As a reference, a diode without guards has been designed (A1). Set B again consists of a basic

structure with six p^+ guards (B2); n^+ and p^+ intraguards have been added (B1 and B3, respectively). As a reference, a structure with only the n^+ guards has been produced (B4). Baby detectors are surrounded by guards with the A2 design.

This design was based on that already examined in [9], which had already shown some limits, especially regarding the comparability between the different solutions. Now, within each set of devices, distances between corresponding guard pairs are kept constant so that a direct comparison between different layouts is possible. Moreover, in the previous design only the inward field plate option was taken into account, while now the outward field plate option also is considered (A4). In addition, we had previously noticed [9] that the applied potential mainly drops between large guard and first floating guard, with a nonoptimized potential distribution. Therefore, a structure with an increased number of guards and decreased intraguard spacing has been designed (B3) to obtain a better voltage distribution across the guards. These different solutions are to be characterized from the point of view of their breakdown limit to find the best compromise leading to high breakdown voltages taking care of the radiation environment in which they are meant to be employed.

To test the minimum safe distance between the last p^+ implant and the n^+ external well, we designed special edge structures (produced by CSEM). They are 1-mm diameter circular p^+ implants surrounded by an n^+ implant at the edges. The gap between p^+ and n^+ implants can be 25, 50, 75, 100, 150, or 250 μm .

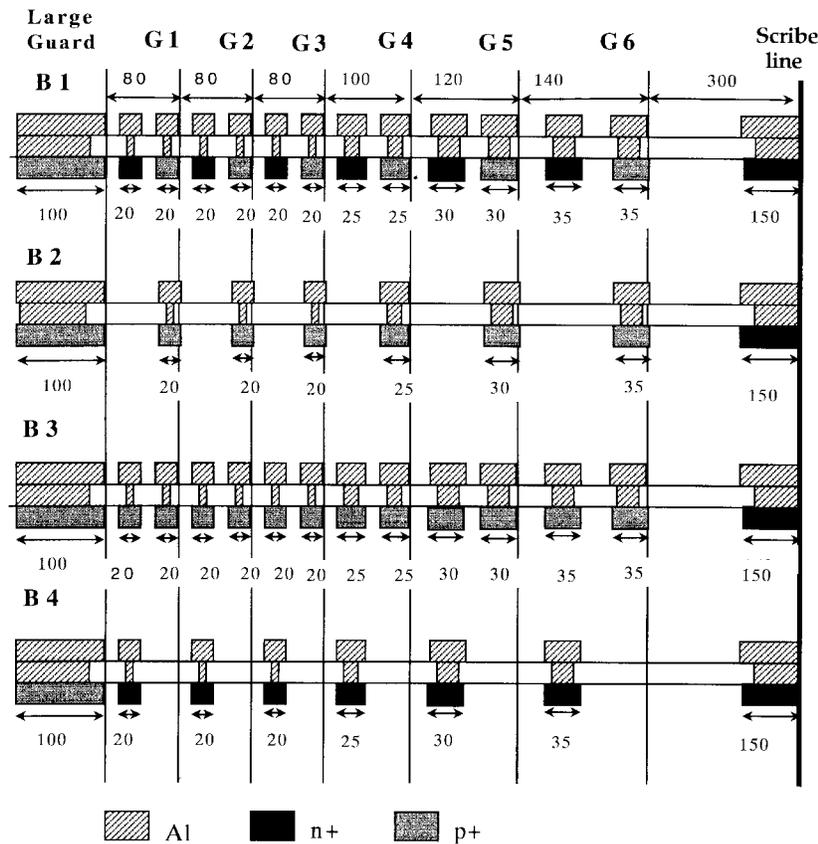


Fig. 2. Set B of multiguards. The large guard is on the left, while the scribe line through the n-well is on the right (distances are expressed in micrometers).

A SiO_2 layer passivates the device surface. Implant contacts are generally in aluminum. For comparison purposes, some ST devices have an Si_3N_4 layer interposed between metallization and oxide; in these cases the contact can be polysilicon or aluminum. The metal contacts on both p^+ and n^+ implants are $6\ \mu\text{m}$ wider than the corresponding implanted regions, with a $3\text{-}\mu\text{m}$ overlap over the junction on both sides. By means of simulations we have seen that this narrow metal overlap leads to a better field distribution in the junction-surface proximities, with meaningful breakdown voltage increase, in agreement with [10]. Its dimensions have been chosen to be large enough according to the technology sensitivity and narrow enough not to have the features of a field plate. In the structures with field plate options the design allows a gap between metallizations of $25\ \mu\text{m}$.

B. Multiguard Structure Characterization

All dc measurements were taken using an HP 4142B picoammeter capable of measuring up to 1000 V. For each set of measurements, the central diode and the large guard were kept grounded, while a variable bias was applied to the backside and current was measured at each terminal. The floating guard voltage can be measured by forcing a zero net current on the corresponding metal contact.

The available devices were characterized to evaluate the breakdown point, V_{BD} , defined as the knee voltage in the I - V log-lin plot. The V_{BD} values for all devices are listed in Table I.

The behavior of the CSEM devices is generally different from that of the ST ones. The latter are available in a smaller number, and a statistical approach is not possible.

Regarding CSEM structures, the highest breakdown value is found for layouts with only p^+ guards, i.e., A2, B2, and B3, showing breakdown voltages often above 1000 V. Lower V_{BD} values, (i.e., below 500 V) are not frequent and should be attributed to localized defects.

Inward field plates (A3) tend to reduce the breakdown voltage (as previously observed [9]), which mainly falls in the range 500–700 V. In most of the devices with outward field plates (A4) the avalanche breakdown point is too high to be measured with our experimental apparatus. Instead, the current starts to increase slowly (this behavior is labeled “*sr*,” *smooth raise*, in the table) also at quite low voltages (~ 400 V). Diodes without multiguards (A1) exhibit variable breakdown voltages, often around 300 V, even if higher values are recorded as well. Structures with n^+ intraguard (B1) have breakdown voltage much lower than B2 devices, usually in the range 400–500 V, while the devices with only n-type guards (B4) feature breakdown voltage in the range 300–350 V.

The plot of the guard voltage versus applied bias (V_G - V characteristics) is shown for an A2 and an A4 device (CSEM) in Fig. 3. A3 devices show characteristics very similar to A2 devices. For each given pair of guards, the inward field plate results connect to the most positive floating guard (i.e., the external one), with the effect of increasing the surface accumulation layer density. In fact, the field plate acts as the

TABLE I
BREAKDOWN VOLTAGES (EXPRESSED IN VOLTS) BEFORE IRRADIATION, FOR
LAYOUTS A AND B MEASURED ON DIFFERENT DEVICES. THE
SCRIPT "sr" INDICATES SMOOTH CURRENT RAISE; C PREFIX
INDICATES DEVICES PRODUCED BY CSEM, WHILE S INDICATES ST

Layout	A1	A2	A3	A4	B1	B2	B3	B4
wafer								
C6xx	400	530	460	460sr	500	>1000	>1000	360
C6yy	690	>1000	400	350sr	490	>1000	>1000	350
C6zz	>1000	>1000	700	>1000	480	400sr	>1000	360
C679	>1000	>1000	720	420sr	480	>1000	770sr	330
C682	520	>1000	685	460sr	540	>1000	>1000	375
C685	800	>1000	790	400sr	490	>1000	650sr	350
C1714	320	>1000	480sr	550sr	440	600	>1000	335
C1715	520	>1000	690	760sr	420	520	>1000	320
C1721	325	560	530	720 sr	-	700 sr	>1000	300
C7122	360	950	630	740sr	400	590	>1000	310
C1728	780	>1000	970	490sr	-	-	-	-
C1729	300sr	440	290	>1000	-	-	-	-
C1758	290	400	400	>1000	360	430	>1000	280
C1759	240	450	350	>1000	320	420	>1000	250
S1m	>1000	160sr	660sr	470	330	250	810	190
S1p	740sr	800	550	230	-	-	-	-
S1mn	>1000	>1000	550	320sr	-	-	-	-
S5m	>1000	860sr	650sr	320sr	340sr	670sr	770sr	245sr
S5p	>1000	>1000	320sr	320sr	-	-	-	-
S5mn	580sr	460sr	130sr	920 sr	-	-	-	-

gate of a p-MOSFET shorted to the corresponding source. This does not have strong effects on the potential barrier between adjacent guards determining the punch-through onset, since the latter is mainly a bulk phenomenon [11]. On the other hand, it has negative consequences on the breakdown as it forces the potential difference between adjacent guards to drop across a narrower surface depletion layer. The behavior of outward field plates is completely different. In this case, the gate of the equivalent p-MOSFET is shorted to drain. This produces a decrease in the accumulation layer density in a way which is dependent on the potential drop across the oxide and on the oxide charge density. As a result, the silicon surface underneath the field plate can be weakly accumulated, depleted, or even inverted, clearly corresponding to the p-MOSFET turned off, subthreshold, or saturation regimes, respectively. This behavior is mainly controlled by the "source-to-drain" potential drop which is different within each pair of guards [12]. This is reflected in the guard voltage curves (Fig. 3), which are lower in devices A4 with respect to devices A2. Operation of outward field-plate structures has been shown to depend strongly on the degree of coverage of the gap with the metal plate [12]. For a completely covered device, the voltage drop between adjacent guards equals the corresponding MOS transistor threshold voltage, which differs not so much within each pair of guard rings and is almost independent on the gap size. Such a voltage drop is, however,

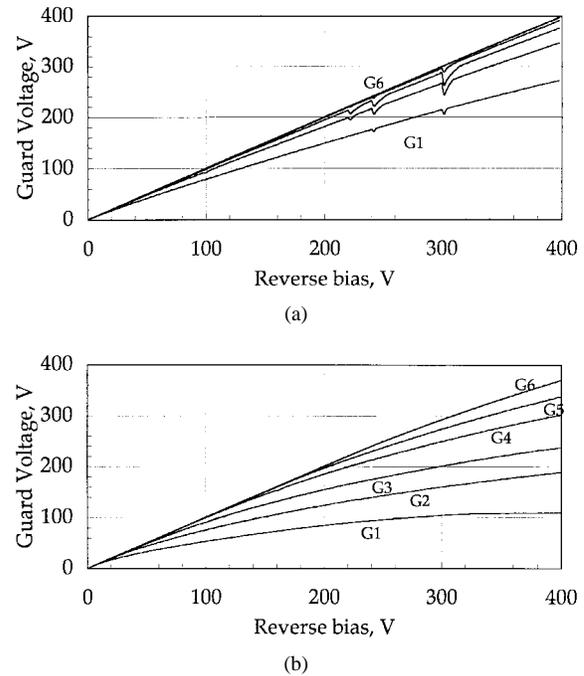


Fig. 3. (a) Guard voltage versus reverse bias curves for A2 and (b) A4 structures.

too low for guarding operation, at least in the unirradiated state. In partially covered devices, as is the case of A4 devices, the gap introduced between the plate and the following guard contact provides an additional potential barrier, making the device suitable for guarding operation. The potential on the top of the uncovered oxide becomes, however, very crucial in determining the device behavior. For instance, a charging up of this potential at the field-plate potential can reduce the onset voltage dramatically. The stability of the oxide surface potential depends, in turn, on the properties of the passivation layer as well as on the environmental conditions. This makes such structures particularly prone to long-term instability problems in humidity environments [12].

In addition, the guard voltage distribution curves are scarcely reproducible when devices come from different wafers, being sensitive to process-induced oxide charge variations. As observed in the figure for A4, there is a potential difference between the last guard (G6) and the backside indicating that the diode SCR has reached at least that position. Due to the extension of the SCR to the device edges, it is possible that excess current is drained to the large guard resulting in the smooth current raise observed in the $I-V$ curves.

The effect of the intraguard is different according to the doping type. As previously observed [9], n^+ intraguards are shorted to adjacent external p^+ guard potential. Therefore, the voltage difference between two neighbor p^+ guards drops across a narrower distance with a resulting decrease of the breakdown voltage in comparison with the case without intraguards. To contrast this detrimental effect we have increased the intraguard spacing with respect to the previous design [9]. The same considerations hold true for B4 devices, where the applied voltage is forced to drop entirely between the large guard and the first n-type guard.

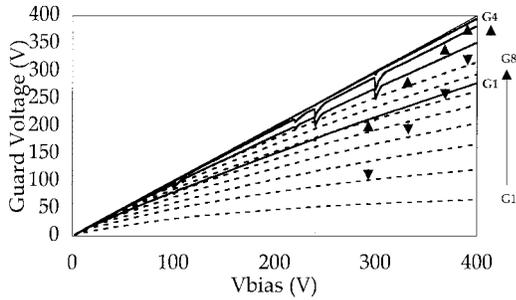


Fig. 4. Guard voltage versus reverse bias curves for a B2 (solid) and a B3 (dashed) structure. The arrows indicate guards in the two devices at the same distance from the main junction.

As already observed (see Table I), devices with p-type guards have high breakdown voltage. In particular, a large number of guards with a narrow gap produce a more balanced distribution of the applied voltage along the surface, as shown in Fig. 4, where V_G-V curves relative to a B2 and a B3 device are plotted together. Arrows indicate guards at the same distance from the large guard. The potential drop in B2 is larger than in B3. In layout B3, distances between p⁺ guards are reduced to less than a half with respect to B2. A stronger reduction is consequently observed in the punch-through voltages which approximately scale with the square of the source-to-drain distance [11], [13].

The different trend observed for the ST devices can be partially ascribed to lower oxide charge and to larger oxide thickness. As a result, there is a lower potential drop between neighbor guards with respect to the CSEM case for the same layout. This is reflected on the breakdown characteristics: devices with only p⁺ guards (A2, B2, B3) often show smooth current raises at relatively low voltages, while the devices with outward field plates show the smooth raise at even lower voltages (around 300 V in most cases). The high voltage breakdown in devices without protection (A1) is again attributed to the low oxide charge and to the field plate effect of the small metal overlap on a thicker oxide. The poor performances observed in devices A3, B1, and B4 manufactured by ST could be attributed to a technology which is not yet optimized for high voltage operation. No extra effect has to be attributed to the differences in the contact metallizations.

C. Edge Device Characterization

$I-V$ characteristics were measured on cut devices to determine the breakdown point of each structure. The measurements suffered from instability problems, probably due to environmental variations affecting the surface [14]. In fact, a large section of the surface is not metallized, and it results in being very sensitive to the environment conditions (humidity and temperature) much more than in the case of multiguard devices. In some cases, after a few voltage sweeps a considerable breakdown voltage reduction was observed, probably due to stress-induced oxide damage. On the other hand, measurements performed with low voltage ramp rate were reproducible.

The breakdown values are shown in Fig. 5 as a function of the gap width. The breakdown tends to increase with the gap width up to a saturation value reached at gap widths larger than 150 μm . The plateau value ranges from ~ 550 V to ~ 300 V. This latter value is reached at high substrate doping and oxide charge concentrations.

The solid lines in the figure are obtained from the models proposed by Baliga [1] for a punch-through diode (vertical lines), i.e., a p⁺-n-n⁺ diode operating in full depletion and for a cylindrical p⁺-n junction (horizontal lines). In detail, at narrow gap widths the SCR easily reaches the edge n⁺ implant and cannot widen anymore: the model for the punch-through diode applies. At large gap widths, the SCR is free to extend laterally, hence the model for a cylindrical junction applies. This picture is only ideally true, as the SCR lateral width is limited by the surface accumulation layer.

The agreement between the two theoretical models and the experimental data is qualitatively good at the extrema of the considered interval. In the intermediate region the limits of both models are evident. The model for the punch-through diode is monodimensional and we applied it in the direction parallel to the surface, between the two implants. But, the SCR widens also in the direction of the substrate. This becomes important when the gap width is not negligible with respect to the substrate thickness. On the other hand, the model for the cylindrical junction, even if two-dimensional, is unable to account for the passivation layer with its trapped charge and the small metal overlap. Moreover, the cylindrical approximation of a p⁺-n junction could be far from the actual junction shape.

Simulations have been performed by means of DESSIS, a program part of the ISE-T-CAD package, which solves both Poisson and electron-hole current continuity equations. The transport model adopted considers the drift-diffusion expressions for the hole and the electron current densities. Impact ionization is modeled according to van Overstraten and De Man [15], while mobility degradation at the Si-SiO₂ interface is accounted for by activating the transverse electric-field dependence in the mobility model. Homogeneous Neumann boundary conditions are imposed on top of the uncovered oxide. As input data, geometrical values for implant shapes were taken from the manufacturer data, while for other parameters we used values obtained from laboratory measurements. The simulation results (full symbols in Fig. 5) are in good agreement with the experimental data over the full range of distances. This proves again the analytical model limits.

D. Irradiation Test Results

1) *Gamma Irradiation*: We irradiated some multiguarded diodes and a baby detector in the ⁶⁰Co gamma-cell at CNR-FRAE laboratory in Bologna. All samples were kept under bias during irradiation, in overdepletion, but well below the breakdown point, as specified in Table II. The total dose received in 4 h was 1 Mrad (Si).

The overall effect of the irradiation is a reduction of the breakdown voltage. The ionizing radiation produces an increase of the positive charge trapped into the oxide. This

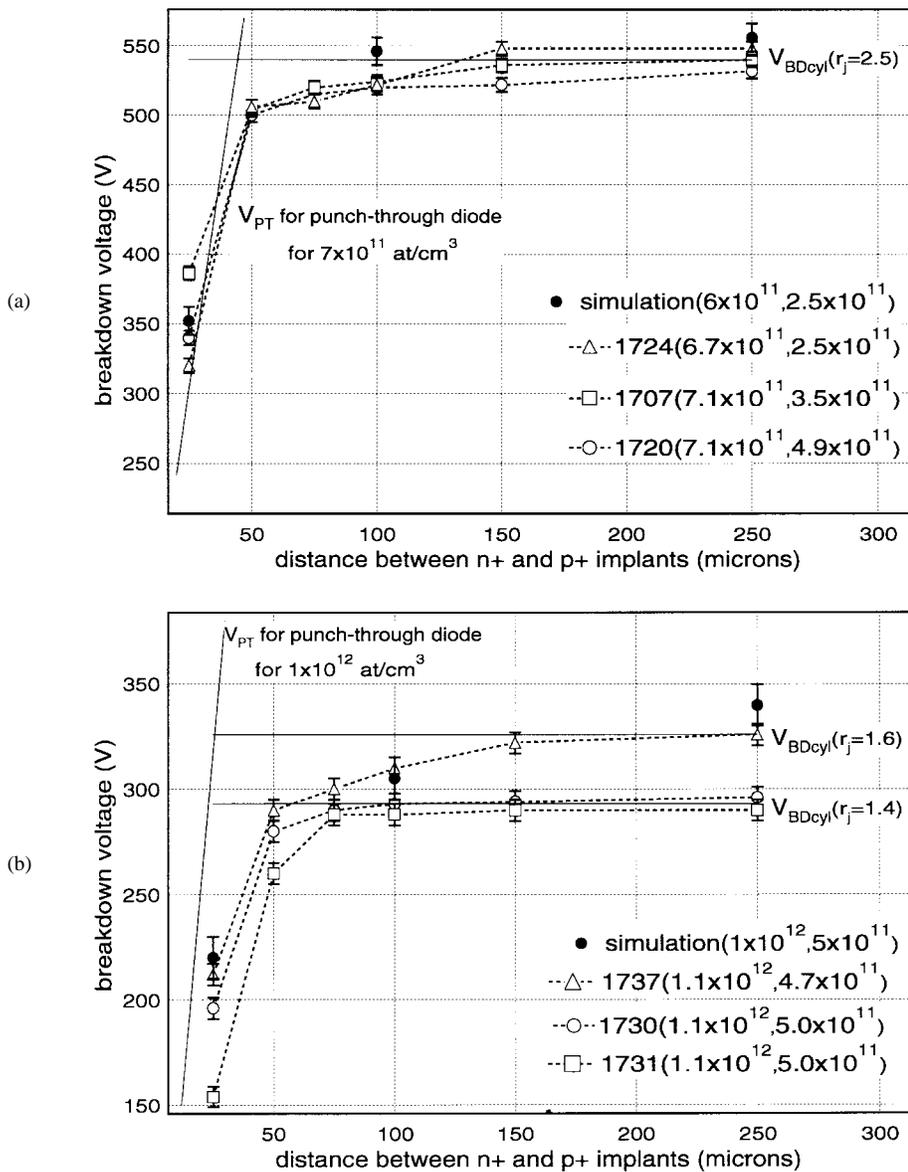


Fig. 5. (a) Breakdown voltage obtained by experimental results (open symbols and dotted line), model predictions (straight solid lines), and simulations (full symbols). Curves were grouped according to the device substrate doping concentration: $N_D \sim 7 \times 10^{11}$ cm⁻³ and (b) $N_D \sim 1 \times 10^{12}$ cm⁻³. In parenthesis N_D (expressed in cm⁻³) is specified as a result of measurements together with the surface charge (cm⁻²). r_j is the fitting parameter for the cylindrical junction model.

drives the silicon surface to strong accumulation, causing a reduction of the junction SCR width at the surface [7]. As a consequence, the electric field at the surface increases with a resulting breakdown voltage reduction. Soon after irradiation, this effect is particularly evident in devices without protection (A1) or in those showing poor breakdown performances before irradiation, such as devices with n-type intraguards (B1, B4) or inward field plates (A3). In both cases, V_{BD} lowers to 200–300 V.

Irradiation induces the smallest breakdown voltage decrease on devices featuring only p⁺ guards. Only in one case does the breakdown drop to ~ 450 V in irradiated A2 samples, with a recovery after about a week up to 830 V. Generally, values over 700 V were observed. The baby detector, which has an A2 guard structure, shows a decreased breakdown from 1000 to 500 V. Even in this case V_{BD} returns to 630 V after eight

days. Irradiated B2 devices have slightly lower breakdown voltages, but always above 400 V. On the other hand B3 (12 p⁺ guards) devices show the best behavior—they always keep $V_{BD} \geq 1000$ V.

A different trend is established in A4 devices (outward field plates) where the knee voltage on the I - V curve actually tends to increase up to values approaching 1000 V. In this case the enhanced accumulation layer reduces the SCR width so that it cannot easily reach the device edges.

No particular effect seems to be due either to the technology or to the value of the applied bias, the final breakdown voltages being quite independent of these two factors.

2) *Proton Irradiation:* We irradiated all A and B devices from the same wafer (C1714) with 24 GeV/c protons at CERN-PS. Considering 0.6 as the damage factor for 24 GeV/c protons [16], the normalized fluence was 1.8×10^{13} p cm⁻², chosen

TABLE II
BREAKDOWN VOLTAGES (EXPRESSED IN VOLTS) BEFORE, IMMEDIATELY AFTER, AND EIGHT DAYS
AFTER γ IRRADIATION. THE SCRIPT "sr" INDICATES SMOOTH CURRENT RAISE OR "SOFT BREAKDOWN"

wafer	device	Bias during irradiation	BD before	BD after	BD 8 days after
Cz	A1	265	> 1000	340	380
	A2	265	< 1000	450	830sr
	A3	265	700	270sr	400sr
	A4	265	>1000	>1000	800sr
C1715	A1	400	520	damaged	-
	A2	400	>1000	>1000	860
	A3	no bias	690	580	540
	A4	265	760sr	540	330
S5mn	A1	-	>1000	-	-
	A2	400	>860sr	750	180sr
	A3	-	650sr	-	-
	A4	265	320sr	950sr	>1000
S5p	A1	400	>1000	340	200
	A2	400	>1000	900	250
	A3	265	320sr	420	280
	A4	265	320sr	900	>1000
S5n	A1	400	480sr	660	200
	A2	400	460sr	820sr	250sr
	A3	265	130sr	200	220sr
	A4	265	920	>1000	>1000
Cz	B1	265	480	360	365
	B2	265	400sr	400	500
	B3	400	>1000	>1000	>1000
	B4	200	320	280	275
C1715	B1	265	420	310	330
	B2	265	520	400	360
	B3	400	>1000	>1000	>1000
	B4	200	320	240	180
S5mn	B1	265	340sr	200	280
	B2	265	670sr	>1000	>1000
	B3	400	770sr	930	>1000
	B4	200	245sr	240	180
C1703	Baby	400	>1000	480	650

in order to study the device behavior close to the substrate inversion point. The equivalent dose was 0.8 Mrad.

After proton irradiation, the breakdown voltage generally decreases. Devices without protection or with B4 multiguards show the breakdown at around 250 V. Devices A2, A3, B1, and B2 tend to set their final breakdown at around 400 V. In all cases this value is much lower than the preirradiation one. The B3 device shows the highest V_{BD} value after proton irradiation. As shown in Fig. 6, the breakdown, above 1000 V before irradiation, lowers to 630 V just after irradiation, with an almost complete recovery 21 days later. As seen after γ

irradiation, device A4 has a higher breakdown voltage after proton exposure.

Guard voltage distribution curves after proton irradiation are shown in Fig. 7 for an A2 device. They should be compared to those in Fig. 3(a). The trend of the V_G-V curves after irradiation is completely different as a potential drop is now present between all guards and the backside also at very low applied voltage with no evidence of the punch-through onset. This is due to the change in the substrate doping concentration leading to type inversion; the substrate effectively behaves as a p-type and the conduction mechanism between guards is not ruled

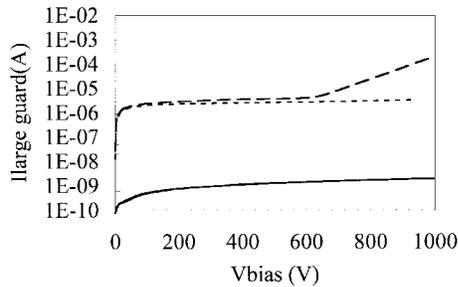


Fig. 6. I - V characteristics before irradiation (solid), just after proton irradiation (dashed), and after partial annealing (dotted) for a B3 device.

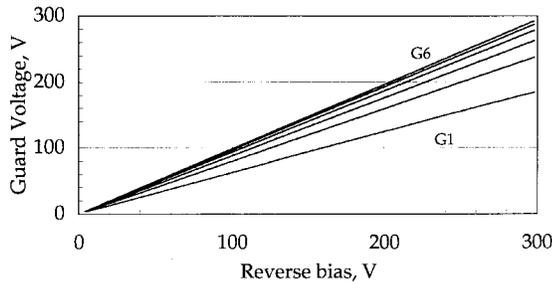


Fig. 7. V_G - V characteristics after proton irradiation for an A2 device.

anymore by punch-through mechanism. A resistive behavior is recognizable as curves show a linear trend. Nevertheless, the potential barrier between pairs of guards is still kept high by the enhanced electron layer at the surface. In this way current conduction from the edges is avoided.

The effects observed on the breakdown are similar to those seen after γ irradiation and they must be attributed to surface damage induced by ionizing protons. Being the substrate after irradiation close to the inversion point, it can be considered as an intrinsic material. Therefore, the electric field is mainly determined by the accumulation layer of electron underneath the surface, thus resulting very sensitive to the surface damage.

III. SIMULATIONS

Optimization of a multiguard structure via two-dimensional numerical simulation is a computationally prohibitive task, requiring in principle all the intraguard distances and guard widths to be changed simultaneously and all the resulting possible combinations to be simulated up to avalanche breakdown.

In this work, two simplified structures were simulated by using DESSIS (see Section II-C for a brief description of the models adopted): the first one consists of a simple diode with a single floating p^+ guard. Both implants (diode and floating guard) are $20\text{-}\mu\text{m}$ wide, while the distance between them has been varied from 10 to $60\text{ }\mu\text{m}$. The second structure was obtained by inserting an n^+ guard between the main junction and the p^+ guard. Such an n^+ implant is $20\text{ }\mu\text{m}$ wide and equally spaced from the two junctions. In this case, the gap between p^+ guards has been varied from 40 to $60\text{ }\mu\text{m}$. The simulation domain has been extended laterally to rule out any border-related punch-through effect. The purpose of this work was to find the optimum distance for the single floating guard achieving the highest avalanche breakdown voltage and to study the effect of the insertion of an intraguard.

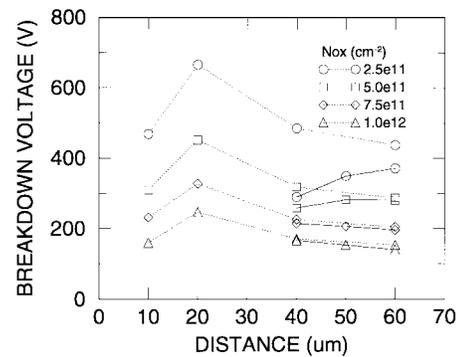


Fig. 8. Simulated avalanche breakdown voltages as a function of the distance between diode and p^+ guard for the structure with a single floating p^+ guard (dotted) and for that with an n^+ intraguard between diode and p^+ guard (solid). Data are reported for different oxide charge density values.

Simulations were performed for different values of the fixed oxide charge density. More specifically, the considered charge density values range from $2.5 \times 10^{11}\text{ cm}^{-2}$ to $1.0 \times 10^{12}\text{ cm}^{-2}$, the latter value being close to the radiation damage saturation level [17]. By increasing the oxide charge density, the damage induced by ionizing radiation can be taken into account, at least in a first-order approximation. As a matter of fact, in the real experimental conditions the irradiated devices are usually under bias. Therefore, the voltage drop across the oxide is different according to the position (e.g., close to or far from the metallization/field plates). As a result, oxide charge build up is not uniform, as assumed in the simulations for simplicity.

Simulation results are summarized in Fig. 8, where the avalanche breakdown voltage is reported as a function of the distance between the p^+ implants for different oxide charge densities and for the two different structures considered. The device with a single floating p^+ guard has an optimum spacing of $20\text{ }\mu\text{m}$, giving the highest breakdown voltage regardless of the oxide charge value.

Such optimal spacing corresponds to a characteristic electric field distribution, as shown in Fig. 9. In fact, in this case the two local maxima of the electric field, located, respectively, at the external side of both the diode and the p^+ guard, have basically the same value. For narrower gaps, the highest electric field peak is on the external side of the floating guard junction, while, for spacings wider than $20\text{ }\mu\text{m}$, it is at the diode junction. As a consequence, the avalanche breakdown voltage sharply decreases by decreasing (down to $10\text{ }\mu\text{m}$) or increasing (up to $40\text{ }\mu\text{m}$) the gap. Further enlarging the gap from 40 to $60\text{ }\mu\text{m}$ results in a smoother reduction of the breakdown voltage.

As expected, the avalanche breakdown voltage is sensitive to the oxide charge density as well. At the optimal spacing, it decreases from 680 to 250 V while the oxide charge density is increased from $2.5 \times 10^{11}\text{ cm}^{-2}$ to $1.0 \times 10^{12}\text{ cm}^{-2}$.

Finally, the n^+ intraguard does not practically influence the breakdown value for positive oxide charge values greater than $7.5 \times 10^{11}\text{ cm}^{-2}$; however, at lower values its insertion does reduce the breakdown voltage. Such behavior can be explained as follows. The n^+ intraguard is at the same potential of the external p^+ guard, minus the small junction

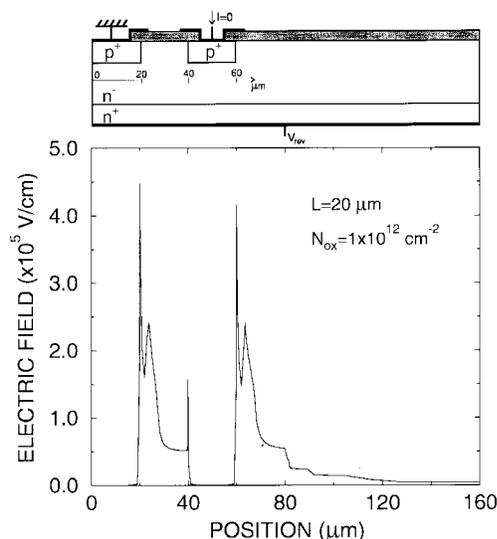


Fig. 9. Surface electric field distribution at breakdown. The oxide charge density is 10^{12} cm^{-2} . In the upper part of the figure, a sketch of the simulation domain (not to scale) is also shown.

forward bias. This happens because the punch-through current forward biases the $p^+ - n - n^+$ junction consisting of two adjacent guards [9]. Similarly, the surface accumulation layer connecting the n^+ guard to the external p^+ guard is practically at the same potential. As a result, at low oxide charge densities, the n^+ guard actually reduces the distance between diode and p^+ guard over which the surface potential can drop. This increases the local electric field, which, in turn, reduces the breakdown voltage. Such an effect is more pronounced as the gap between diode and p^+ guard (and therefore between the diode and the n^+ intraguard) is reduced. This explains why the breakdown voltage decreases for smaller gaps at low oxide charge density. At high oxide charge concentration the n^+ intraguard has little or no influence on the local electric field distribution, and the resulting breakdown voltage does not appreciably differ from that relative to the structure with the p^+ guard only. However, the n-stop layer implies a minimum distance between diode and p^+ guard wider than $20 \mu\text{m}$, thus not allowing for the optimal spacing.

The analysis considered in this section has focused on two simplified, single-guarded structures (with and without an n^+ intraguard). Such an analysis, although not allowing straightforward generalizations to the multiguard problem, provided some useful indications which can be exploited in the design of multiguards. First of all, it is pointed out that the optimal gap between the large guard and the first p^+ floating guard is wide enough to be compatible with the technology constraints commonly adopted for the fabrication of silicon detectors, this fact justifying the effort made to determine it. Otherwise, such a distance could simply be chosen as the minimal value allowed by the technology tolerances. Second, it explained why structures with n^+ intraguard behave worse than those without n^+ intraguard.

IV. CONCLUSIONS

In this work we have proved that multiguard structures are effective devices to enhance and control the breakdown voltage of a $p^+ - n$ diode.

A design with a large number of p^+ guards and reduced intraguard spacing has shown the best behavior before and after γ and proton irradiation, as it can well distribute the applied potential across the surface.

Ionizing radiation damage leads to a reduction of the breakdown voltage, due to positive charge trapping into the oxide and enhanced electric field at the junction. This effect dominates also after proton irradiation leading to type-inversion. In this situation, p^+ guards are still isolated by the electron accumulation layer, which mainly controls the electric field distribution at the silicon surface.

We have identified a minimal safety distance of 150 to $200 \mu\text{m}$ between the n^+ implants and the most external p^+ implant.

Numerical simulations have given indications that the optimum spacing for the single floating guard is $20 \mu\text{m}$.

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REFERENCES

- [1] B. J. Baliga, *Modern Power Devices*. New York: Wiley, 1987, pp. 62–100.
- [2] Y. C. Kao and E. D. Wolley, “High-voltage planar p–n junctions,” *Proc. IEEE*, vol. 55, pp. 1409–1414, 1967.
- [3] M. S. Adler, V. A. K. Temple, A. P. Ferro, and R. C. Rustay, “Theory and breakdown voltage for planar devices with a single field limiting ring,” *IEEE Trans. Electron. Devices*, vol. 24, pp. 107–113, 1977.
- [4] B. J. Baliga, “Closed-form analytical solutions for the breakdown voltage of planar junctions terminated with a single floating field ring,” *Solid-State Electron.*, vol. 33, pp. 485–488, 1990.
- [5] A. Bischoff, N. Findeis, D. Hauff, P. Holl, J. Kemmer, P. Klein, P. Lechner, G. Lutz, R. H. Richter, and L. Strüder, “Breakdown protection and long-term stabilization for Si-detectors,” *Nucl. Instrum. Methods Phys. Res.*, vol. A326, pp. 27–37, 1993.
- [6] L. Evensen and A. Hanneborg, “Guard ring design for high voltage operation of silicon detectors,” *Nucl. Instrum. Methods Phys. Res.*, vol. A337, pp. 44–52, 1993.
- [7] T. P. Ma and P. V. Dressendorfer, *Ionising Radiation Effects in MOS Devices and Circuits*. New York: Wiley, 1989, pp. 149–232.
- [8] U. Biggeri, E. Borch, M. Bruzzi, S. Lazanu, and Z. Li, “CV and Hall effect analysis on neutron irradiated silicon detectors,” *Nucl. Instrum. Methods Phys. Res.*, vol. A338, pp. 330–334, 1997.
- [9] M. Da Rold, A. Paccagnella, A. Da Re, G. Verzellesi, N. Bacchetta, R. Wheadon, G.-F. Dalla Betta, A. Candelori, G. Soncini, and D. Bisello, “Radiation effects on breakdown characteristics of multiguarded devices,” *IEEE Trans. Nucl. Sci.*, vol. 44, pp. 721–730, 1997.
- [10] G. Gramegna, F. Corsi, E. Cantatore, M. Cuomo, D. De Venuto, C. Marzocca, G. V. Portacci, A. Vacchi, V. Manzari, F. Navach, S. Beole, G. Casse, P. Giubellino, L. Riccati, and P. Burger, “Use of fielded plate in a linear silicon drift detector (SDD),” *Nucl. Instrum. Methods Phys. Res.*, vol. A360, pp. 110–112, 1995.
- [11] A. Paccagnella, D. Bisello, M. Da Rold, Yu. Gotra, and P. Benetti, “Study of punch-through characteristics in irradiated MOSFET’s,” *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 2511–2516, 1994.
- [12] B. S. Avset and L. Evensen, “The effect of metal field plates on multiguard structures with floating p^+ guard rings,” *Nucl. Instrum. Methods Phys. Res.*, vol. A377, pp. 397–403, 1996.
- [13] S. Sze, *Physics and Technology of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981.
- [14] A. Longoni, M. Sampietro, and L. Strüder, “Instability of the behavior of high resistivity silicon detectors due to the presence of oxide charges,” *Nucl. Instrum. Methods Phys. Res.*, vol. A288, pp. 35–43, 1990.
- [15] R. Van Overstraeten and H. De Man, “Measurements of the ionization rates in diffused silicon p–n junctions,” *Solid-State Electron.*, vol. 13, pp. 583–608, 1970.
- [16] RD48 Status Rep., CERN/LHCC 97-39, June 20, 1997, Linstroem, RD48, private communication.
- [17] R. Wunstorf, “Radiation hardness of silicon detectors: Current status,” *IEEE Trans. Nucl. Sci.*, vol. 44, pp. 806–814, 1997.