Sensor Concepts for Pixel Detectors in High Energy Physics

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Abstract

Different approaches in the design of pixel sensors for various experiments in particle physics are reviewed. A short outlook of potential development directions for future experiments is also given.

1 Introduction

Hybrid pixel detectors consist of a thin, segmented silicon sensor with highly segmented integrated readout chips connected to it via the bump bond technique. The sensor is segmented into pixels of about $0.02\,\mathrm{mm}^2$ area and the readout chip is subdivided into pixel unit cells matching the sensor pixels. While the R&D effort is focused mainly on the challenging readout electronics and bump-bonding technique, less attention was initially given to the sensor. For the first generation pixel detectors, the proven technique of silicon strip detectors was merely adapted. The need of a very high level of radiation tolerance in the LHC experiments however triggered an extensive R&D program both for strip and pixel sensors, with the pixel sensors requiring the highest degree of radiation hardness. This paper reviews pixel sensor concepts for various environments in high energy physics experiments in the past and present, and discusses the limitations of the different approaches. The requirements of possible future experiments are shortly mentioned and some fields of present research are summarized.

2 First Generation Pixel Detectors

The first generation pixel detectors e.g. the ones of WA97 [1] and DELPHI [2] used DC-coupled "p^+ in n" sensors as sketched in fig. 1. The pixels are p^+-implants in an n-type substrate forming a pn-junction. As the p^+-side's metallization is directly connected to pixel-implants, no cost driving features like poly-resistors or large area capacitors have to be implemented. The backside is connected via an ohmic contact realized by an overall

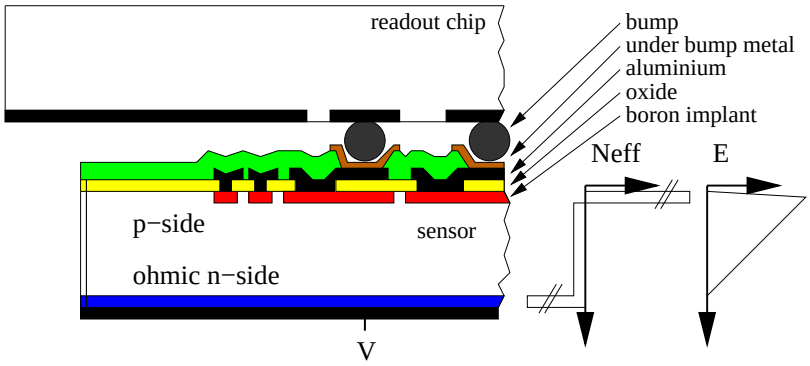


Figure 1: Cross section of a p^+ in n pixel detector. The effective doping and the electric field at full depletion voltage is also indicated. The dimensions do not scale correctly.

n^+-implant and an aluminization. These sensors require only four mask layers and – most important – no photolithographic step on the backside. Therefore they are called single sided.

When applying a positive backside voltage the sensitive space charge region starts to grow from the *pn*-junction on the structured side of the sensor until it is stopped by the high dose n^+-implant at the backside. The field created by the junction in the fully depleted state is sketched on the right side of fig. 1. It's maximum is close to the collecting electrode while it vanishes at the backside contact. Therefore the device can be operated partially depleted. This might become necessary if the backside is mechanically damaged and an extension of the depletion zone into the damaged region would lead to an unacceptable current increase.

Since radiation hardness is not an issue in the applications discussed in this section, usually a low doped float zone *n*-substrate with a resistance of several $\mathrm{k\Omega\,cm}$ is used. This leads to a full depletion voltage below $50\,\mathrm{V}$. The high voltage stability of the devices is not critical and guard ring structures with one or two rings are sufficient. Due to the low operation voltage, the small distance of one bump diameter between the sensor edge being on backside potential and the grounded edge of the readout chip is uncritical and no sparking between both parts has been observed in this kind of devices.

2.1 Pixel Layout

A possible layout of a pixel cell is sketched in fig. 2. It consists on a rectangular p^+-implant, with the metalization covering almost the whole implanted area, and a broad contact opening. The pads for bump bonding are located at the end of the pixel and are often arranged in a mirrored geometry as indicated.

Whereas the pitch is given by the required spatial resolution and the bump pad position by the design of the readout chip, the implant width is a "layout decision". It determines

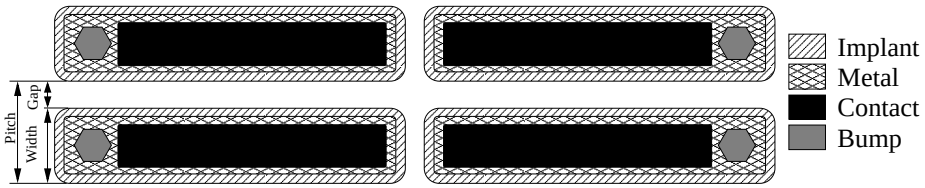


Figure 2: Possible layout of a pixel cell.

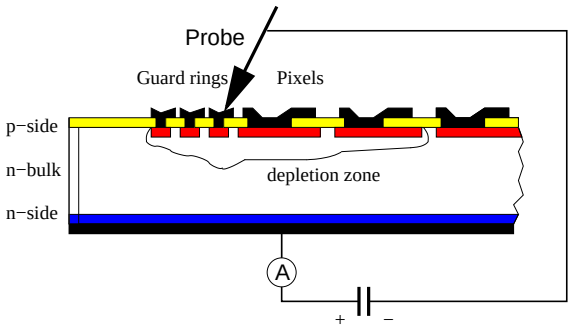


Figure 3: IV-setup for a simple p^+ in n sensor.

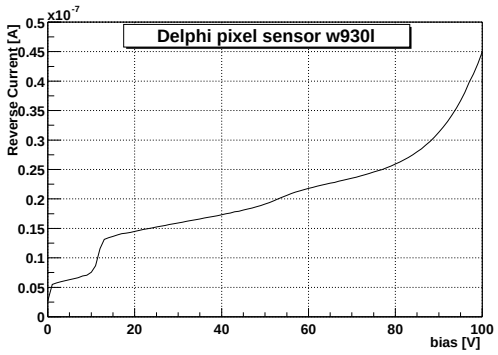


Figure 4: Measured IV-characteristic [4].

the capacitance between neighboring pixels. The noise in the pixel preamplifier is mainly determined by it's capacitive load. The total capacitance of a pixel is dominated by the capacitance towards it's neighbors. This can be decreased by increasing the gap width. In order to keep the pitch unchanged, the implant width has to be decreased at the same time. In "strip like" pixel geometries with a large aspect ratio as shown in fig. 2, only two of the neighbors contribute significantly to overall capacitance and therefore only the gap indicated in fig. 2 needs to be maximized. However if one tries to push this approach too far the charge collection will be affected and the signal could be out of time [3].

2.2 Sensor Testing

Usually pixel detector modules consist of several readout chips placed on one sensor. After this procedure all the pixel cells on the sensor are grounded via the bump bonds and the chips. As the chips are the most expensive part of a pixel detector, it is of interest to test the sensor before attaching it to several readout chips. The easiest method for testing sensors is to take an IV-curve, since already small damages lead to an increase of the leakage current, if they are inside the space charge region. In order to fully deplete the sensor, all pixels must be contacted. As it is impossible to contact even a small fraction of the roughly 50 000 pixel cells in a highly segmented sensor with a probe card, e.g. in the DELPHI

experiment only the guard current was measured as sketched in fig. 3. A measurement performed during the DELPHI module production is shown in fig. 4 [4]. In the first part the current displays the usual square root like behavior as the depletion zone grows just below the directly biased guard rings. During the measurement the depletion zone expands also laterally and punches through to the first row of pixels at about $12\,\mathrm{V}$. From this voltage the depletion zone also grows below these pixels as indicated in fig. 3 and the depleted volume is much larger leading to a higher current level as visible in fig. 4. The punch through between $50\,\mathrm{V}$ and $55\,\mathrm{V}$ to the next pixel row is less clearly visible. The breakdown at roughly $100\,\mathrm{V}$ is probably not due to any sensor damage but due to high fields in the punch through regions. As at $100\,\mathrm{V}$ only a small part of the sensor is depleted due to lateral punch through, most pixels and a large fraction of the backside remain untested. However, this method is capable to detect "obviously faulty" devices that show a much higher current and different shape of the characteristic. At the end of the module production of the DELPHI pixel detector about 8 % had to be rejected because of high leakage current and 5 % due to high noise [5]. Which fraction of those could have been avoided by more advanced sensor testing is unknown.

3 Radiation Induced Effects in Silicon

In the experiments discussed up to now radiation hardness was not required. This changes when moving to high rate experiments with hadrons. In the context of LHC (and SSC) radiation induced effects have been systematically studied since the late 1980s [6, 7, 8, 9, 10]. Usually a distinction between crystal damage in the sensor volume (*bulk damage*) and effects at the interfaces (*surface damage*) is made.

3.1 Bulk Damage

As silicon and other semiconductors are crystals it is expected that they will suffer from radiation defects. High energetic particles will not exclusively interact with the electron cloud producing the electrical signal but also with the nuclei often displacing them out of the lattice. This produces crystal imperfections that may be electrically active and change the electric properties of the material. In the inner regions of high rate hadronic experiments the concentration of crystal defects will after some years of operation exceed the initial substrate doping. At this moment the material properties will be mainly determined by the defects. Even though it is not yet possible to correlate all changes in the operation parameters of the sensors with specific microscopic defects, these changes have been studied in detail. This allows a prediction of all the important sensor parameters for a given radiation scenario [8, 11, 12, 13]. The most important quantities influenced by bulk defects are shortly summarized in the following.

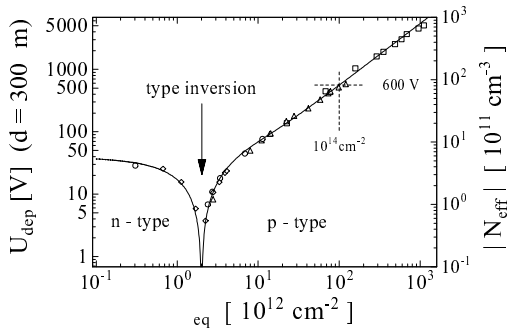


Figure 5: Change of the full depletion voltage of a $300\,\mu\mathrm{m}$ thick silicon sensor [8].

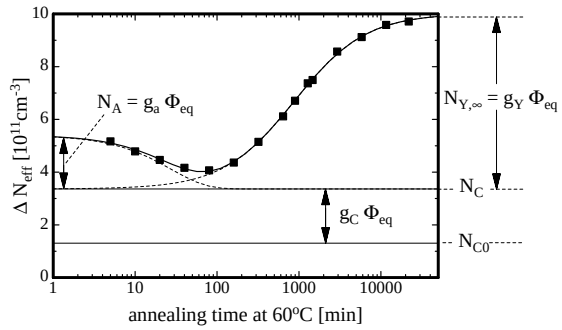


Figure 6: Annealing behavior of the effective space charge after irradiation with a fluence of $1.4 \times 10^{13}\,\mathrm{cm}^{-2}$ [12].

Leakage current: The leakage current increases proportionally to the fluence of the charged particles. As the leakage current is strongly temperature dependent, irradiated sensors have to be cooled during operation in order to prevent thermal runaway which might be destructive.

Full depletion voltage: The full depletion voltage changes during irradiation as shown in fig. 5. In the first part up to several $10^{12}\,\mathrm{cm}^{-2}$ it is decreasing as the process of donor removal is dominant. At a higher fluence the creation of radiation induced defects with negative space charge becomes dominant, leading to a space charge sign inversion (also called type inversion). The depletion zone after this fluence starts to grow from the n^+-side of the sensor. The total space charge mainly caused by the radiation induced defects is referred to as the effective doping concentration. As it increases proportionally to the fluence, the full depletion voltage also increases. In order to keep the sensitive volume constant, the applied voltage has to be steadily increased up to values of several hundred volts. As the energy levels associated to those defects are located deep in the band gap, they do not contribute to the conductivity, and irradiated silicon features only the intrinsic conductivity. The effective doping concentration displays a complex annealing behavior shown in fig. 6, commonly described by the Hamburg model [12, 14]. After irradiation the effective doping concentration decreases to a minimum (stable damage, $g_C\Phi$ in fig. 6) reached after about one week at room temperature (beneficial annealing) and slowly increases afterwards (reverse annealing). In order to slow down this increase, irradiated detectors have to be kept cool also outside running periods.

Extensive work has been done to evaluate whether the post-irradiation properties can be affected by specific impurities other than boron, phosphor or arsenic. It was found that an enrichment of the silicon substrate with oxygen, which is believed to capture vacancies in stable and electrically neutral point defects, leads to a superior post-irradiation performance

for samples irradiated with charged hadrons [13, 15]: The increase of the full depletion voltage after irradiation induced space charge sign inversion is reduced by about a factor of 4 compared to non-oxygenated float zone material. Furthermore reverse annealing is slowed down by a factor of two and its amplitude is reduced. As the main fluence in the innermost part of the experiments at hadron colliders, where pixel detectors are commonly located, is due to charged pions, the use of oxygenated material is recommended there.

Trapping Radiation induced defects act also as charge trapping centers. Traps are mostly unoccupied in the depletion region due to the lack of free charge carriers and can hold or *trap* parts of the signal charge for a time longer than the charge collection time and so reduce the signal height. The inverse trapping time is proportional to the concentration of traps and therefore proportional to the fluence. Trapping times in irradiated silicon have been measured for electrons and holes [16]. Holes are more prone to trapping than electrons and therefore the collection of electrons is preferred for applications in very harsh radiation environment. A complex model has been built to predict the dependence of the charge collection efficiency on the trapping time and the electric field inside the sensor [11]. For most of the tracking devices used in particle physics this effect is much less of a problem than the radiation induced effects mentioned above. However if the particle fluence approaches or even exceeds $10^{15}\,\mathrm{cm}^{-2}$ the charge collection efficiency degraded by trapping will be the limiting factor of silicon devices [17].

3.2 Surface Damage

In silicon the surface region is also sensitive to radiation. The term surface damage summarizes all defects in the covering dielectrics, e.g. the silicon oxide and the interface between the silicon and the dielectric. As the crystal structure of silicon oxide is highly irregular, displacement of single atoms due to irradiation does not lead to macroscopic changes. Ionization in the oxide however is not fully reversible and may cause steady changes of the interface properties. One consequence of ionization in the oxide is the build up of a positive fixed oxide charge that saturates after some kGy at a value of about $3 \times 10^{12}\,e/\mathrm{cm}^2$ [18, 19, 20]. This oxide charge changes the electric field in the silicon bulk close to the surface and induces a compensating electron accumulation layer in *n*-type silicon and a depletion layer in *p*-type material.

A further effect of radiation is the generation of interface states leading to a surface generated current when the space charge region reaches the surface. This contribution to the dark current is proportional to the area not covered by the pixel implants [20].

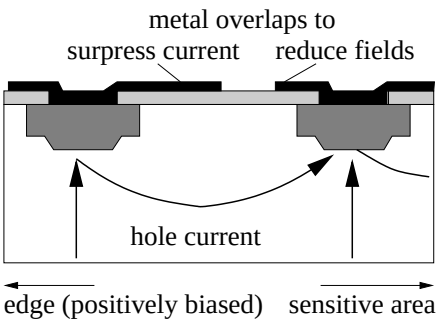


Figure 7: Schematic cross section of a possible guard ring design with metal overlaps according to [22, 23].

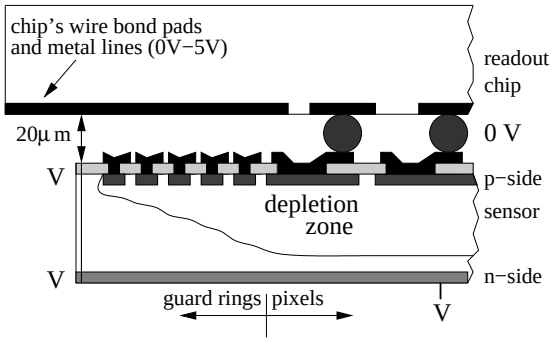


Figure 8: Depletion region below guard rings and potential of surfaces and edges.

4 Radiation Hardness of p^+ in n Sensors

In an unirradiated p^+ in n device the depletion zone is growing from the junctions on the structured p^+-side. After the space charge sign inversion the depletion zone starts to grow from the the unstructured backside. As long as the depletion region has not reached the surface, all pixels on the p^+-side are connected via the inverted undepleted bulk material. As this material has a poor conductivity, it is transparent to fast signals. This means that "p^+ in n" sensors irradiated over the point of inversion deliver spatial information even when operated slightly under-depleted [21]. However the signals become very small with increasing under-depletion and therefore it is not advisible to rely on this feature in an experiment. The use of p in n sensors can only be recommended if the radiation and temperature scenario predicts a full depletion voltage which can realistically be applied. Therefore radiation hardness becomes equivalent to high voltage capability. In the coming sections some measures to increase the high voltage stability are discussed.

4.1 Guard Rings

The purpose of a multi guard ring structure is to establish a gradual voltage drop between the sensitive region on ground potential and the cutting edge on backside potential. It avoids high fields and subsequent breakdown at the device edge and prevents the space charge region from reaching the heavily damaged edge region. Floating rings bias themselves via the punch through mechanism. The potential drop between the rings can be influenced by their spacing and a metal overlap. Field plates directed outwards reduce the electric field at the implant edge. This is a technique used in power electronics since the late 1960's [24]. However it also reduces the punch through voltage between two neighboring rings if it covers too much of the gap. Therefore these overlaps are usually kept relatively small as indicated in fig. 7. A field plate directed towards the sensitive region suppresses the punch

through hole current and increases the punch through voltage [22]. This can be understood in terms of a *p*-MOSFET with the gate (large field plate directed inwards) connected to the source (the outer of each two rings). Such geometries are therefore preferred over designs using outwards directed field plates [23].

The number of guard rings necessary depends on the maximal bias voltage targeted. If a uniform potential drop between the rings is aimed for, the spacing has to increase from the inner to the outer regions. Although there is always some pressure to have a small edge region in order to minimize dead material, a useful rule-of-thumb is to foresee a distance of roughly three times the wafer thickness between the cutting edge and the sensitive region.

It has to be mentioned that a reliable edge termination can also be obtained with only two guard rings, one very close to the edge on backside potential and one very close to the sensitive region on ground. Both rings have to be connected via a highly resistive (but not perfectly isolating) passivation covering the whole oxide surface in between to guarantee a well defined and gentle potential drop. However such a passivation is not offered by most sensor vendors and the use of such a concept has to be carefully discussed with the processing foundry.

4.2 Module Concept

The high voltage capability is not only determined by the sensor itself but also by system aspects. In most module concepts followed for hybrid pixel detectors, the wire bond pads of readout chips overlap the sensor edges as indicated in fig. 8, and the chip approaches the sensor to a distance of about $20\,\mathrm{m\mu}$. The size of this gap limits the high voltage capability of the device as the breakdown voltage of air (of the order of $1.2\,\mathrm{V/\mu m}$ [25]) can easily be reached. This is one of the reasons why in applications requiring high voltage operation a double sided concept with guard rings on the backside is chosen.

4.3 Limits in Radiation Hardness

Due to their simplicity, p^+ in *n* sensors are the first choice for most detector applications, especially those where radiation damage is not an issue as for example WA97 [1], DELPHI [2] or Alice [26].

In these systems high resistive silicon is used and the operating voltage is always far below 100 V. However, if one wants to exploit the limits in radiation hardness of this sensor type as done by silicon strip detectors e.g. in the CDF layer 00 [27], ATLAS [28] or CMS [29], one needs operation voltages of $300 - 500\,\mathrm{V}$ and is faced with the limitations given by the module design as mentioned above. This problem might be solved by avoiding overlapping chips or adding on top of the sensors a dielectric layer that stands several hundred volts. The MCM-D technique [30] seems a good candidate for such a solution (section 6). If it is found to be practical, operation of p^+ in *n* sensors can easily be extended

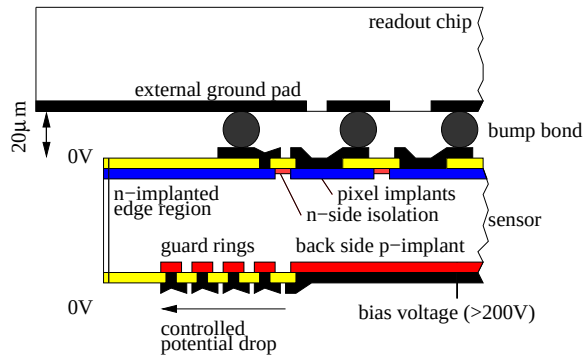


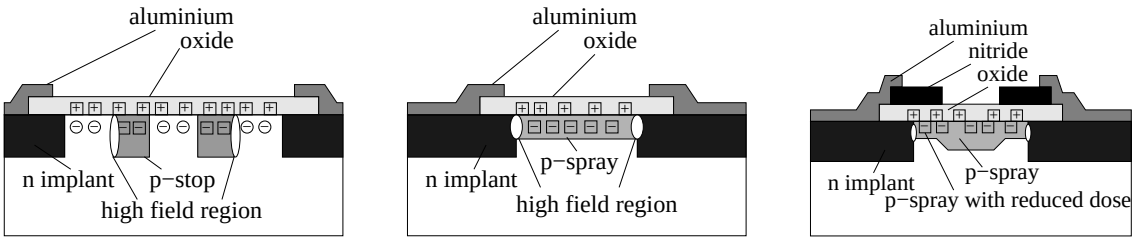
Figure 9: Guard ring concept of n^+ in n sensors. The bias voltage is applied on the sensor's junction side. This side of the sensor contains also the multi-guard ring structure providing a controlled potential drop towards the edge. The whole sensor side facing the readout electronics can be held at ground potential.

into the range of $2-3\times10^{14}\,\mathrm{n_{eq}/cm^2}$. The limitation for such devices is given firstly by the rise of the full depletion voltage and secondly by signal loss due to trapping.

5 High Luminosity Experiments with Hadrons

The requirements of the LHC experiments ATLAS [31] and CMS [32], and of BTeV [33] at FermiLab in terms of radiation hardness cannot be fulfilled with the previously discussed p^+ in n sensors. At the end of the targeted lifetime of the detector, a full depletion voltage of more than $1000\,\mathrm{V}$ is expected. As the maximum bias voltage foreseen is in the order of $600-700\,\mathrm{V}$, an under-depleted operation of the sensors is required for a significant part of their lifetime. To cope with this problem, all experiments mentioned have chosen the n^+ on n concept for their pixel sensors. The pixels consist of n^+-implantations in high resistivity n-type silicon while the *pn*-junction is located on the sensor's backside, surrounded by a multi guard ring structure as indicated in fig. 9. After radiation induced space charge sign inversion, the depleted region starts to grow from the n^+-side and the device can be operated partially depleted, if full depletion cannot be reached any more. Furthermore, the double-sided processing of n^+ in n detectors allows a guard ring concept which keeps all sensor edges at ground potential and avoids the risk of disruptive discharges to the very closely spaced front-end chip. This can be achieved by placing the multi-guard ring structure on the p-side, i.e. the sensor's backside. The outer region of the n^+-side containing the pixel cells is covered with a large n^+-implant, grounded externally via the readout chip. For the design of the guard rings the considerations from section 4.1 are still valid.

In comparison with standard p^+ in n sensors, n^+ in n sensors are roughly twice as expensive due to the need for double sided processing and inter-pixel isolation. Furthermore,



(a) *p*-Stops (b) *p*-Spray (c) moderated *p*-Spray

Figure 10: Isolation techniques for adjacent n^+-implants. Fixed (□) and free (◯) charge carriers are indicated. The field maxima are located at the lateral *pn*-junctions

a lower yield compared to single sided devices has to be expected and an effective sensor testing before bump bonding is very important. As a direct probing of all pixel cells is not possible, some biasing structure has to be integrated onto the sensor itself. Possible implementations are discussed in the context of the pixel designs in section 5.2.

5.1 Inter Pixel Isolation

In contrast to the *p*-side, were the isolation of the adjacent p^+-implants is provided by the omnipresent electron accumulation layer, exactly this accumulation layer electrically connects the n^+-implants of the *n*-side if no precautions are taken. Isolation is usually provided by a boron implant between the pixels forming a lateral *pn*-junction. Depending on the dose this isolation implant is called either *p*-stop or *p*-spray.

5.1.1 *p*-Stop Isolation

In double sided strip detectors, a common technique is to introduce a high dose p^+-implant between the strips as shown in fig. 10a. This is done by an additional photolithographic step. The alignment of the *p*-stop mask with respect to the n^+-pixels is critical as an overlapping of the two high dose implants would result in Zener breakdown. The minimum spacing between two n^+-implants is therefore limited by the necessary alignment tolerances. The advantage of this technique is that a typical dose of about 10^{14} boron ions per square centimeter will in any case guarantee good isolation also after the radiation induced build-up of a positive surface charge, and the adjustment of the implantation dose is not at all critical.

The electric field close to the lateral *pn*-junction was numerically calculated using a two dimensional device simulation package [34]. The un-irradiated device has a very low oxide charge, resulting in a low electric field. The value of the oxide charge increases after a small irradiation dose of below $20\,\mathrm{kGy}$ to its saturation value, resulting in an accumulation

of electrons close to the surface and consequently in a strong increase of the electric field. The potential of the *p*-stop depends on the implant geometry, the backside bias and the substrate doping. As the two latter values also are very high in a highly irradiated sensor, the potential difference between n^+-pixels and the p^+-stops increases with ongoing irradiation, leading to an additional, but less drastic, increase of the electric field. The operation of devices featuring *p*-stops in a strong radiation field is limited by their decreasing high voltage capability.

5.1.2 *p*-Spray Isolation

If the dose of the boron implant is matched to the saturation value of the oxide charge which is of the order of $3 \times 10^{12}\, e/\mathrm{cm}^{-2}$, the boron concentration is so small, that an overlap of the boron implant with the pixel's n^+-implant does not lead to breakdown. Therefore the mask separating both implantations can be omitted and the whole surface is then covered by the medium dose boron implant. At the places of the pixels the high dose n^+-implant is not compensated. Because of the missing mask this technique is called *p*-spray isolation [34]. The absence of a photolithographic step is a cost advantage and also permits narrow spacing between neighboring n^+-implants, as there are no alignment tolerances between two different masks to be kept.

The point of maximal electrical field is the lateral *pn*-junction between the isolating boron implant and the n^+-pixels as indicated in fig. 10b. The un-irradiated device shows the highest electrical field and therefore the lowest breakdown voltage in its life cycle. With the increase of the oxide charge to its saturation value the shallow *p*-spray layer moves into the depleted state and the electric field decreases. The lowest electric field is reached when the boron implant matches exactly the saturation value of the oxide charge. However if the implantation dose is too low the isolation might not be sufficient. Therefore one usually chooses an implant dose a bit higher than necessary to prevent failure in case of fluctuations in the production process. With the following increase of the effective substrate doping the electric field shows an uncritical increase. Therefore these devices are characterized by an improved high voltage performance after irradiation.

In order to improve the pre-radiation high voltage stability of *p*-spray devices while keeping their good post-irradiation behavior, the *moderated p*-spray technique [35] has been developed. Here the *p*-spray implant is performed later in the production process. A topography on the wafer's surface, as for example obtained with a nitride layer shown in fig. 10c, will then be reproduced in the doping profile as indicated. The boron dose in the middle of the gap between two pixels can be chosen high enough to ensure inter pixel isolation, e.g. twice the expected saturation value of the surface charge. At the same time the boron dose in the surrounding of the lateral *pn*-junction can be optimized for the best high voltage performance which is reached when the dose is close to the expected saturation value of the surface charge. As the nitride layer is a standard step in the process of many detector vendors this technology in most cases does not need an additional pho-

tolithographic step. However, the freedom to design very small gaps between the pixel implants is limited in the moderated *p*-spray technology as the moderation is only effective if the layer of the moderated *p*-spray dose has a minimum width of about $3 - 5\,\mu\mathrm{m}$.

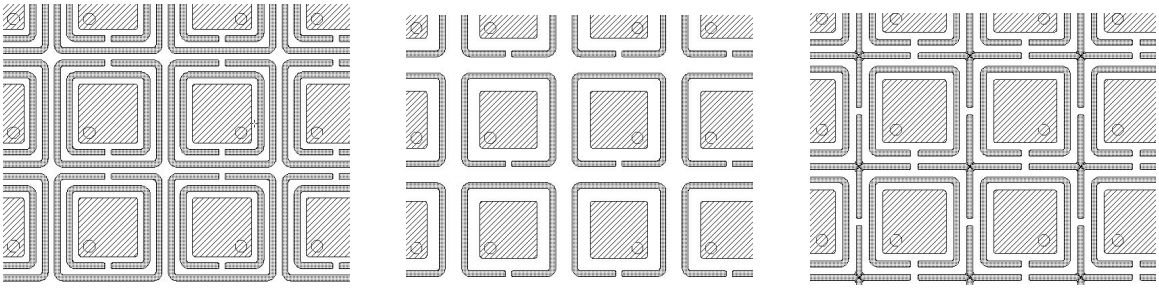
5.2 Pixel Layouts

The layout of the pixel cell depends strongly on the *n*-side isolation technique. Therefore both methods are discussed separately.

5.2.1 Layouts with *p*-Stops

When designing a *p*-stop isolated device, most attention is paid to the geometry of the *p*-stops. For strip detectors numerous geometries have been evaluated [36, 37]. However in pixel devices "atoll" like structures are preferred in order to avoid local defects affecting the whole array [38]. P -stops provide a very good isolation. However, in some situations a high resistive connection between the pixels is desirable, for example to perform IV-tests of the devices on wafer level, or to hold unconnected pixels close to ground when the full depletion voltage is exceeded. In case of an ohmic connection between neighboring pixels, the maximum value is determined by the maximum acceptable voltage drop between pixels and the leakage current, leading to a value of the order of $1\,\mathrm{G}\Omega$. The lower limit of the inter-pixel resistance is given by the requirement of preventing a significant signal distribution to the neighbor channels within a typical shaping time of 25 ns. This leads to a lower limit of the resistance of about $1\,\mathrm{M}\Omega$. Resistors can be implemented by openings in the *p*-stop implants surrounding every pixel cell, which leave room for a conductive electron accumulation layer. The value of the resistance depends on the length and the width of this path. Different possible resistor geometries shown in fig. 11 have been evaluated [39, 40, 41].

The value of the resistance depends very strongly on the backside voltage as shown in fig. 12. At low voltages the current flows mainly through the undepleted bulk. When the space charge region reaches the *n*-side, the pixels are separated from each other and the current has to pass through the electron accumulation layer forming the resistor. This leads to an increase of the resistance as seen in fig. 12 around $150\,\mathrm{V}$ (one *p*-stop ring). When the bias voltage is increased further the resistance first grows slowly for a while before increasing very steeply above $200\,\mathrm{V}$. This is indication of pinch-off, since with further over-depletion the potential difference between *p*-stops and the n^+-implants increases and a field is growing from the *pn*-junction between *p*-stops and bulk also in the lateral direction. The width and height of the "plateau" region between 150 and $200\,\mathrm{V}$ depends strongly on the *p*-stop geometry. In the "one-ring-design" (fig. 11(b)) it is well developed with a width of almost $50\,\mathrm{V}$ at roughly $1\,\mathrm{M}\Omega$. Consequently it is possible to over-deplete all pixels by $50\,\mathrm{V}$ using two probe needles, one placed on the *p*- side diode and the other on the *n*-side guard ring. This allows for a reliable sensor testing. In the "two ring design" shown in



(a) Two *p*-stop rings (b) One *p*-stop ring (c) One *p*-stop ring plus a cross

Figure 11: Layout of pixels with three different open *p*-stop geometries [40, 41]

fig. 11(a) the width of the path is much narrower and the pinch off appears much earlier. A plateau of the inter pixel resistance is hardly visible and therefore such a design does not allow testing [41].

After irradiation the inter-pixel resistance saturates at values of several GΩ almost independently of the design. Although unbonded pixels float to high potentials with respect to their neighbors, no harmful effects have so far been observed. There is no correlation between missing bump bonds and noisy pixels in irradiated samples [40, 41].

At bias voltages of several hundred volts as required in the LHC environment the current usually starts to depart from the square root like behavior [42]. At the same time the number of noisy channels starts to increase dramatically to unacceptable levels [43, 41]. This is probably due to avalanche breakdown at the *p*-stop edges and has also been observed in strip detectors [44]. Several measures to improve this behavior have been proposed. The design with only one *p*-stop ring (see fig. 11(b)) shows less dramatic current increase than the others tested [45] which can be explained by the smaller gaps between the n^+-implants. As the inter-pixel resistance is also matches the requirements for sensor testing, similar designs are used for further studies [46]. Other possibilities to improve the high voltage capability are field plates [47, 48] or a reduction of the *p*-stop dose [41].

5.2.2 Layouts with *p*-Spray

Due to the "missing" mask for the inter pixel isolation, the designs of *p*-spray isolated *n* in *n* pixels look quite similar to those of *p* in *n* devices. So the design shown in fig. 2 could be interpreted as a *p*-spray isolated *n* in *n* device if the implant would be labeled as *n*-type. However, the conducting *p*-spray layer, not shown in the layout drawings, covers the inter-pixel region and must be kept in mind.

The inter-pixel capacitance can be decreased by increasing the gaps between pixel,

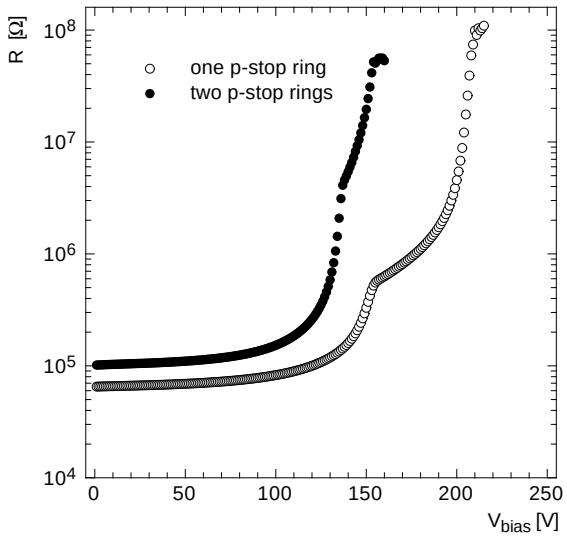


Figure 12: Bias dependence of the inter pixel resistance for the two designs shown in fig. 11(b) and 11(a) [40, 41].

however other considerations favor small gaps. Since the most important requirement to n^+ in n sensors is radiation hardness, the devices have to be optimized for high voltage operation. In order to achieve this, the electric fields have to be kept as small as possible. Therefore the potential difference between the p-spray layer and the pixel's n^+-implant must be limited, as the lateral pn-junction is the most critical spot in these devices in terms of electrical breakdown. The potential of the p-spray is determined by the largest distance between neighboring n^+-implants anywhere on the device. These are usually the diagonal gaps in the regions where four pixels join. In conclusion the use of the smallest gaps still compatible with noise requirements is recommended (typically 15 - $20\,\mu\mathrm{m}$).

The technological possibility to realize even smaller gaps between the n^+-implants (typically $5\,\mu\mathrm{m}$) can be used to implement a punch through bias grid as shown in fig. 13. In an un-irradiated sensor all pixels are connected with each other and to the bias grid through the bulk, as long as the bias voltage applied is below full depletion. When the full depletion voltage is exceeded, all n^+-implants are isolated by the p-spray layer and the leakage current of each pixel has to flow to the bias grid through the depleted bulk via thermo-ionic emission. Due to the narrow spacing the potential difference between a pixel and the bias grid cannot exceed more than a few volts and the grid can be used to bias all pixels. An IV-curve taken with two probe needles is capable to detect most frequent failures, e.g. scratches or spikes anywhere in the sensitive volume. After bump-bonding the bias grid is out of function because the pixels are biased via the readout chip. For this reason no additional noise has been observed in pixel detectors using this feature in contrast to irradi-

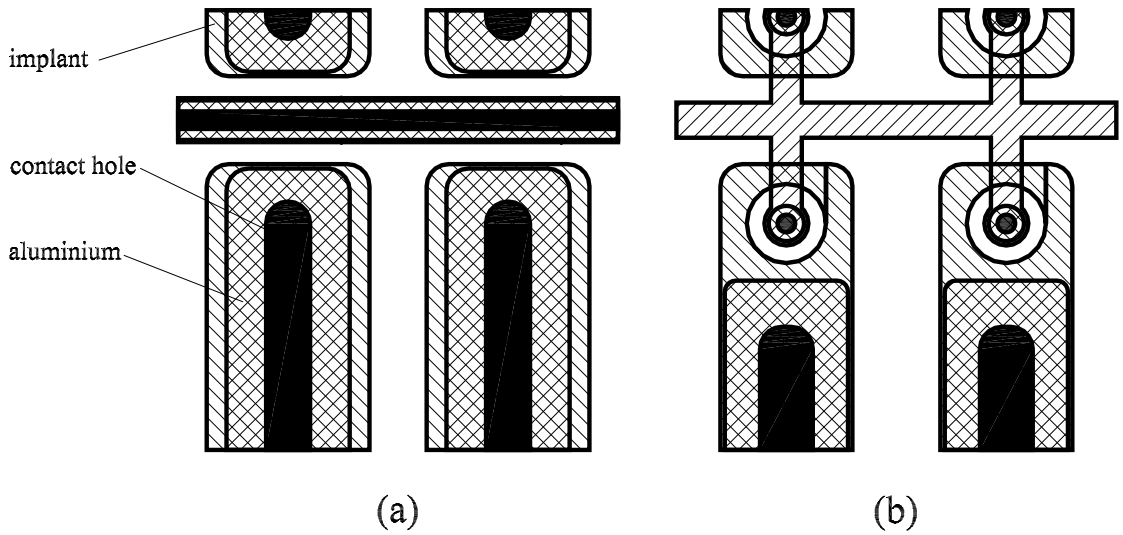


Figure 13: Two possible implementations of a punch through bias grid [43].

ated silicon strip detectors with punch-through biasing [49, 21]. In case of a missing bump bond the unconnected pixel is kept close to ground potential by the bias grid and will not affect the neighbors. The bus line of the bias grid will collect some signal charge, which will be lost, and the particle detection efficiency will be reduced. It is therefore desirable to minimize the area covered by the bias structure.

The implementation shown in fig. 13a is the most simple design with least requirements to the production process. There are no small structures that could approach the limits of the technology and all metal areas are underlayed with an implant. So even pinholes in the oxide would not cause harm. In the design shown in fig. 13b the area affecting the charge collection is minimized. The implantation of the bias structure is shrinked to a small bias dot placed inside the pixel. Surrounding the bias dot with the pixel implant guarantees that the signal generated in the region between the pixels is not lost to the grid. The bus in-between the pixels is just a metal line. Test beam measurements which such devices show a particle detection efficiency above 99 % in the un-irradiated state [50] and above 95 % after irradiation with $10^{15}\,\mathrm{n_{eq}/cm^2}$ [51]. However, such a design is more demanding concerning the fabrication process.

For devices featuring moderated *p*-spray the design considerations are similar. Due to the alignment tolerances and in order to effectively reduce the electric field with a lower boron concentration, a certain minimal distance between the pixel's phosphorus implant and the nitride edge has to be provided. If one tries to implement a bias grid according to fig. 13a one would obtain a too large punch through voltage between the grid and the pixels because of this limitation. However the design shown in fig. 13b can be translated into a

moderated *p*-spray design. The gap between the pixel implant and the bias dot must be filled completely with the full dose *p*-spray. This is possible because the conducting boron layers between the pixels and in the bias structure are electrically isolated and can have different potentials. In the region between the pixels the potential difference between the *p*-layer and the pixels' n^+-implant is higher due to the larger gap but "buffered" by the moderated *p*-spray. The gap between the bias dot and the pixel is very small and therefore the potential difference between the *p*-layer and the pixel-implant is much lower and moderation in this area is not necessary. The pre-radiation breakdown voltage is strongly improved compared to the standard *p*-spray [43, 52] while the good post-irradiation behavior is maintained.

5.3 Limits in Radiation Hardness

The limit of radiation hardness is given by the reduction of signal height. As this degradation is a steady process it is not possible to give a strict rule when a sensor becomes unusable. For the readout electronics used in ATLAS and CMS typically a signal of about 5000 electrons per m.i.p. is required to detect the particle with an efficiency of above 95 %.

The reduction of the signal is caused by the increase of the effective space charge and trapping. The former can be compensated up to a certain level by increasing the operating voltage. Here the limit is given more by practical considerations. In principle it is possible to build sensors with a high voltage capability of more than $1\,\mathrm{kV}$. Trapping can be reduced by collecting electrons, which are less prone to trapping than holes, and by high bias voltages causing shorter collection times. But ultimately trapping will limit the lifetime of silicon detectors.

For the LHC experiments currently under construction a radiation hardness up to a fluence of $1 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ was targeted and reached. This number is currently considered to be the "limit of silicon". However there is no fundamental reason supporting this number and there is interest to push this limit as discussed in the following section.

6 Future Experiments

At the moment two options of future machines are discussed, a linear electron collider and a very high luminosity hadron collider, e.g. a LHC upgrade. They lead to completely different requirements and are discussed separately.

6.1 Very High Luminosity Hadron Collider

Future very high luminosity colliders or a possible LHC upgrade to a luminosity of $10^{35}\,\mathrm{cm^{-2}s^{-1}}$ will require a radiation hardness for tracking devices placed at radii below $10\,\mathrm{cm}$ of up to the order of $10^{16}\,\mathrm{n_{eq}/cm^2}$. In addition the area of devices having to withstand up to

$10^{15}\,\mathrm{n_{eq}/cm^2}$ will increase by at least a factor of three compared to the multi purpose experiments currently under construction. Therefore a cost effective alternative to the n^+ in n pixel detectors must be found.

Both problems are addressed by the CERN-RD50 collaboration [53]. Several approaches to improve radiation hardness of silicon devices are followed [54]. The change of the material properties due to irradiation can be influenced by "defect engineering". For this the crystal defects leading to degradation of the performance must be understood on the microscopical level. Enriching the silicon bulk material with certain impurities, e.g. oxygen, can influence the formation of crystal defects and alter the post-irradiation material properties. Furthermore the operating conditions can be changed concerning the operating temperature [55] or the polarity of the operation voltage [56]. Other device structures e.g. 3-D detectors [57, 58] or ultra thin detectors are considered in order to minimize the drift path of the signal charge which reduces trapping and the voltage needed for full depletion. Other materials like diamond [59] or compound semiconductors are also investigated.

Very high luminosity hadron collider will not only entail a demand for "ultra radiation hard" tracking devices but also heavily increase the need for devices operating in the fluence range up to $10^{15}\,\mathrm{n_{eq}/cm^2}$ currently covered by hybrid pixel detectors with n^+ in n sensors. As these devices are much too expensive to equip tens of square meters, other concepts must be found. The most cost driving features in the present pixel technology are the full coverage of the sensitive area with readout electronics and the double sided sensor processing. The MCM-D technique proposed for integrating the HDI on the sensor [60] can in addition be used to route signals for the case of different pitches on readout chip and sensor [30]. It is conceivable to build "macro pixel" or "mini strip" detectors with a sensor cell size of the order of $1\,\mathrm{mm}^2$ [61, 62]. They could be read out by a small number of pixel chips with a much smaller cell size in the order of $.01\,\mathrm{mm}^2$. The routing between the sensor cells and the inputs of the readout chips could be performed using the MCM-D technique which also allows the integration of other components of a module. As the readout chips can be placed completely inside the active area of the sensor the sensor edges need not be kept on ground potential and a single sided sensor would be possible. Best candidates for such a single sided sensor are probably n-pixels in a p-substrate. Such a sensor collects electrons, would be much cheaper than the currently used n^+ in n sensors, and would not undergo a space charge sign inversion. However as donor removal is not important in these devices, their post-irradiation full depletion voltage will be higher.

6.2 Future Linear Collider

At linear colliders the beams come in "trains" of closley spaced bunches with large gaps in-between, offering enough time for readout. Contrary to hadron colliders, simultaneous data recording and data readout is not necessary, and the instantaneous data rate is modest. These are the ideal conditions for the application of CCD's, which have previously been used very successfully at SLD [63]. Most R&D effort for vertex detectors at linear colliders

is put into such a solution [64, 65]. During the time gaps the primary charge signals are transferred to the edge of the CCD rows, where they are amplified for further treatment and read out. Thus a one-to-one coverage of the sensor area with readout chips, as used in hybrid pixel detectors at hadron colliders, can be avoided. This allows the construction of extremely thin detector modules with an ambitious goal of $0.1\,\%\mathrm{X}_0$ or below [64], mainly determined by the smallest achievable sensor thickness.

Other options are integrated CMOS detectors [66] which combine particle detection, first signal processing and data sparsification on a standard CMOS wafer, and DEPFET/DEPMOS detectors [67, 68], which are processed on high resistive sensor material and integrate only the first amplification stage in every pixel cell.

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