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Design and fabrication of planar guard ring termination for high-voltage SiC diodes

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Abstract

An optimized multiple floating guard ring structure is investigated for the first time as an edge termination method for high voltage 4H-SiC planar devices. Simulations were performed to investigate SiC guard ring termination, and determine the optimum guard ring spacing for planar diodes with up to four floating rings. Simulated optimized designs predicted breakdown values from 40% of the ideal breakdown with a single ring, to 84% of the ideal value for diodes with four rings. Implanted 4H-SiC pn diodes with optimized guard ring designs were fabricated and results correlated to simulation. Experimental breakdown values of 1.2–1.3 kV for guard ring structure with four rings were in good agreement with simulated results. © 2000 Elsevier Science Ltd. All rights reserved.

Keywords: Silicon Carbide; Diode; Edge termination; Guard rings

1. Introduction

Silicon carbide has gained a substantial increase in research interest over the past few years as a base material system for high frequency and high power semiconductor devices. 4H-SiC is the most attractive polytype for power devices due to its wide band gap (3.2 eV), high mobility (950 $cm^2 V^{-1} s^{-1}$), excellent thermal conductivity (4.9 $W cm^{-1} K^{-1}$), and high critical field strength ($\sim 2 \times 10^6$ $V cm^{-1}$). Important for power devices, the 10× increase in critical field strength of SiC allows high voltage blocking layers to be fabricated significantly thinner than for comparable Si devices. This reduces device on-resistance, while maintaining the same high voltage blocking capability. Numerous SiC high power switching devices such as GTOs [1,2], MOSFETs [3,4], pn diodes [5–7], and Schottky diodes [8–11] have been demonstrated with results approaching or exceeding the theoretical limits of Si.

Limiting the potential performance of SiC power devices, however, is the relatively immature development of proper edge termination. As is widely known, high-voltage planar junctions under reverse bias exhibit significantly lower breakdown voltages than one-dimensional theory predicts due to 3-D effects of field crowding at the junction periphery [11]. Specialized edge termination structures must be used to minimize this effect and increase the planar junction breakdown voltages to near ideal values. SiC edge termination is thus critical in order to obtain maximum breakdown voltage and correspondingly minimum on-resistance.

Several different edge termination methods for SiC planar pn junction termination have previously been investigated, field plate extensions [10], junction termination extensions (JTE) [5,8,12], and high-resistivity implanted layers [13]. Field plate structures suffer from an enhanced oxide field near the field plate edge due to

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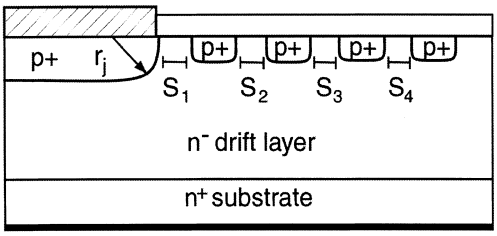

Fig. 1. Schematic diagram of an implanted pn diode with multiple floating guard rings.

the increased critical field strength of SiC, which can result in serious reliability concerns when scaled to higher voltages. JTE methods have produced good results in SiC devices, but often require additional processing steps and precise knowledge of net implant activation percentage.

The floating guard ring structure (Fig. 1) has been widely used in Si technology as an effective means of planar edge termination [14,15]. It is an attractive method of edge termination since it is usually formed simultaneously with the main junction or anode contact, thus saving costly processing steps. The guard ring structure serves to reduce the amount of field crowding at the main junction by spreading the depletion layer past consecutively lower potential floating junctions (rings). A ring becomes biased when the spreading depletion layer punches through to the floating junction. To remain in equilibrium, the ring's potential will follow that of the surrounding material to within the built-in potential of the junction. These independent junctions act to increase the depletion layer spreading, thereby decreasing the high electric field at the main junction. Optimized designs have the electric field shared equally among the main junction and floating rings.

Silicon guard ring planar junctions are predominantly formed by deep diffusion of impurities, which results in a large cylindrical junction radius (x_j). It has been shown [15] that if x_j is large in comparison with the critical depletion width (W_{cpp}), the effects of electric field crowding can be reduced. Additionally, if the ratio of x_j/W_{cpp} is large, optimum ring spacing becomes larger and equally spaced guard rings becomes more effective [16]. This lessens the need for rigorous numerical simulation solutions. Unfortunately, because of the high Si–C bond strength, planar junctions in SiC can only be formed through implantation. Even at high energies, lattice damage and implant time constraints limit junction depths to about 2 μm. For high voltage blocking layers, the r_j/W_{cpp} ratio becomes small, strongly increasing the need for precise ring spacing. We have used numerical simulations to optimize the guard ring spacing for maximum breakdown with minimal area consumption.

2. Guard ring design

The optimization of floating guard ring structures is extremely complex, with the results being strongly coupled to both solution method and grid conditioning [17]. To simulate the potential in the floating guard rings, the hole quasi-Fermi potential must be calculated independently for each p^+-floating ring. Therefore, a coupled solution of both Poisson's equation and both current continuity equations must be used for accurate results.

Simulation results obtained for planar junctions using traditional 2-D simulations have been shown to significantly overestimate the breakdown voltage of planar junctions [18]. In this work, quasi-3D simulations were performed using MEDICI [19] in cylindrical symmetry to account accurately for the effects of three-dimensional field crowding. Device gridding was also determined to play a significant role in convergence stability. Since the gridding requirements vary with device structure and solution method, correct meshing techniques are difficult to relate quantitatively and are often gained heuristically through trial and error. We have found that a minimum gridding of 0.1 μm near floating junctions results in good convergence stability and accurate solutions during subsequent potential updates.

The breakdown voltage of the device was determined when the extracted ionization integral equals to unity. SiC ionization coefficients were determined by fitting the experimental data in [20] to Eq. (1):

$$\alpha_{n,p} = a_{n,p} \exp\left[-\frac{b_{n,p}}{E}\right], \tag{1}$$

where $a_{n,p}$ is the ionization fitting coefficient, $b_{n,p}$ is the critical electric field, and E is the electric field parallel with the current flow. Unlike silicon, holes are the dominant carrier during impact ionization in SiC, and therefore more important in breakdown simulation. The values for the hole ionization parameters a_p and b_p used in these simulations are 5.18×10^6 cm^{-1} and 1.4×10^7 V cm^{-1}, respectively. A 1-D breakdown simulation with these parameters for a variety of punch-through structures is shown in Fig. 2, and is in good agreement with the previously published results [8].

To determine optimum guard ring spacing, the simulations involved an iterative process by which a single ring was first optimized, then additional rings added, and subsequently re-optimized. Fig. 3 illustrates the dependence of the breakdown voltage on the spacing for a single guard ring. It is obvious from this graph that the *exact* spacing of the guard rings can have a significant effect on the breakdown voltage. For a single ring, the optimum junction-to-ring spacing (S_1) is 2.5–3.0 μm. An increase in S_1 shifts the peak field to the edge of the main junction, resulting in a lower breakdown voltage, and

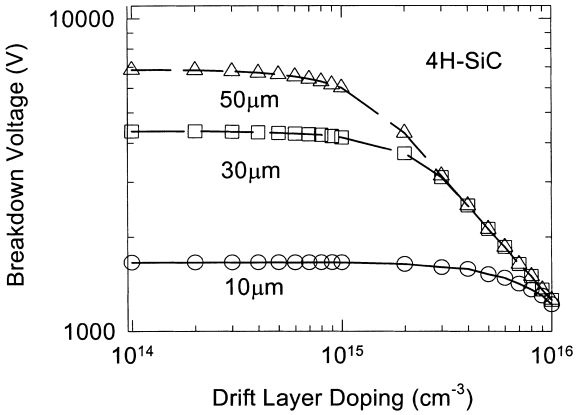

Fig. 2. Simulated 1-D breakdown voltage versus drift layer doping for 4H-SiC p–i–n structures.

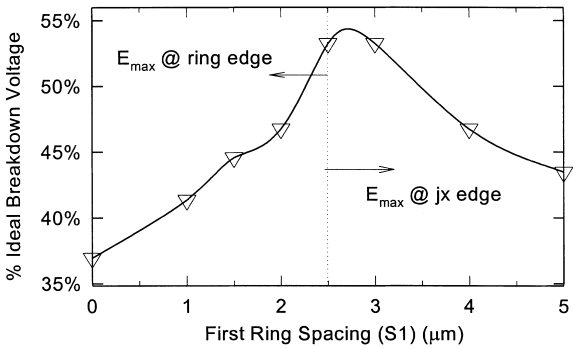

Fig. 3. Simulated increase in breakdown voltage as a function of the first guard ring spacing.

thus stresses the importance of establishing a robust numerical solution strategy for practical device design. If S_1 is decreased, the peak electric field is maintained at the ring edge, but the electric field shielding of the main junction is diminished and the breakdown voltage is lowered.

This process of determining the maximum breakdown voltage while maintaining a uniform electric field profile was repeated for additional rings. Table 1 lists the optimized spacing for a one to four ring design. It was found that with the addition of consecutive rings, the simulated optimum spacing of the previous optimized design is no longer valid due to the increased spreading of the depletion layer and the changing electric field profile. Additional rings added at constant spacing pushes the peak electric field closer to the main junction, requiring a decrease in the spacing of the innermost rings. The optimized profile corresponds to a 10 μm epitaxial layer with $N_D = 1 \times 10^{15}$ cm^{-3}, $S_1 = 1.5$ μm, $S_2 = 1.5$ μm, $S_3 = 2.0$ μm, and $S_4 = 2.5$ μm. The potential and electric field distributions of an optimized four-ring structure are shown in Fig. 4a and b, respectively. The simulated sub-surface field for the optimum profile is shown to exceed the surface field through breakdown, which is important in reducing reliability concerns due to possible charge buildup in the passivation layer. These simulations predict a breakdown voltage of 85% of the ideal 1-D parallel-plane breakdown (1600 V) for this structure with four optimized rings.

As in Si device technology, surface charge resulting from processing conditions or operating stress can significantly alter planar junction breakdown values by either enhancing or restricting depletion layer spreading.

Table 1
Simulated optimum ring spacing for 4H-SiC implanted diodes with a $r_j/W_{cpp} = 0.05$ and ring width of 5 μm

Rings	S_1 (μm)	S_2 (μm)	S_3 (μm)	S_4 (μm)	Ideal (%) V_{BR}
1	3	–	–	–	52
2	2	3	–	–	68
3	2	2.5	3	–	74
4	1.5	1.5	2	2.5	84

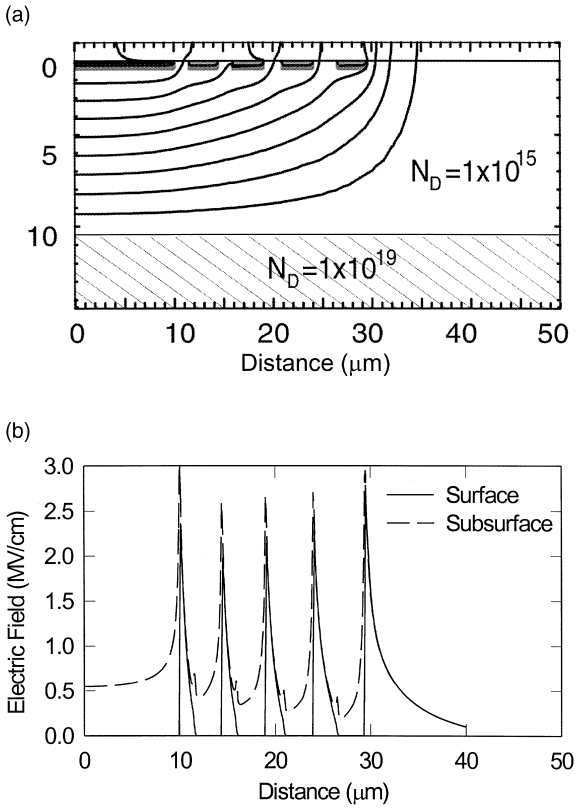

Fig. 4(a,b). Simulated potential and electric field profiles for an optimized four guard ring structure.

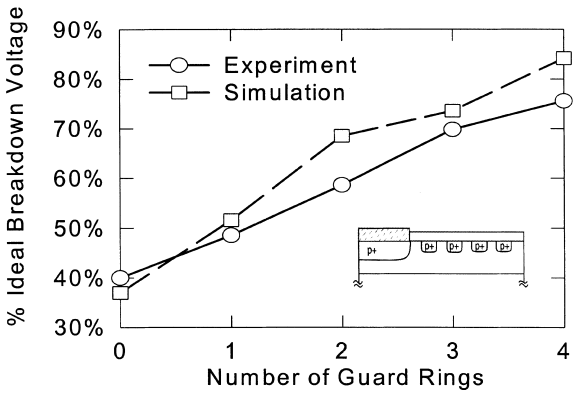

Fig. 5. Simulated change in breakdown voltage due to interface charge for optmized Si [21] and SiC guard ring structures.

This effect depends strongly on charge polarity. For a guard ring structure, this will change the potential at which the depletion region reaches each guard ring, altering the designed field distribution. Since surface charge polarity and density in SiC can easily change with processing conditions and doping type, we have simulated the change in breakdown characteristics due to surface charges for the guard ring structure in order to determine the level of interface charge needed to significantly alter the designed breakdown voltage. As shown in Fig. 5, no significant change in breakdown voltage was seen for surface charges up to 3×10^{12} cm^{-2}. In contrast, Yilmaz et al. [21] reported a significant decrease in simulated breakdown voltage in an optimized six ring Si structure for interface charges between 1×10^{11}–5×10^{11} cm^{-2}. We attribute the increased surface charge sensitivity of Si guard ring structures to the larger ring spacing required for Si devices with the same breakdown rating. A combination of the lower critical depletion width and the shallow junction depth for implanted junctions results in the designed inter-ring spacing being much less for SiC, thereby diminishing the effects of surface charge.

3. Device fabrication

Our optimized floating ring design was experimentally verified with implanted pn diodes fabricated on high quality n$^+$ Cree wafers. The n-type epi-layers were grown at Auburn University by chemical vapor deposition at 1500°C on 5 mm × 5 mm square pieces of n$^+$-doped 8° off-axis 4H-SiC substrates obtained from Cree Research Inc. The thickness of the epi-layers was approximately 10 μm, with a constant carrier concentration of 5×10^{15} cm^{-3} obtained by CV profiling. The p$^+$ anode junction and guard rings were formed by multiple Al implants ranging from 50–260 keV at 700°C. Selective area implantation was performed through a Mo mask patterned by a lift-off procedure. Implant activation and damage annealing was performed at 1700°C for 10 min. After implant activation, the samples were cleaned, a short surface RIE was performed to remove any remaining residue, and a high-quality thermal oxide was grown as a passivation layer. Circular p-type ohmic contact areas were opened with a BOE through a window created by using standard lithography. A thin layer of AlTi was then sputtered and patterned by lift-off prior to the contact anneal at 1050°C for 2 min.

4. Results and discussion

As predicted by simulation, the experimental results for the diodes with implanted guard rings showed a significant improvement in breakdown voltage over those without edge termination. Measurements were made using a Tektronix 371 curve tracer in conjunction with a HP Picoammeter, with the samples immersed in a Flourinert™ solution.

The measured breakdown, normalized to the ideal parallel plane value, is plotted in Fig. 6 for diodes with variable one and two guard ring spacings along with the simulated results. The correlation is good between measured and simulated values except for structures with one ring with a spacing beyond 2 μm. We believe this could be due to a charging of the oxide at the high electric field peaks near the guard ring edge, thus, causing an artificial increase in the depletion layer spreading. This effect is minimized when further rings are added and the potential drop between rings is reduced. Fig. 7 shows the simulated and measured improvement in breakdown voltage for diodes with one to four guard rings. Diodes with a 200 μm diameter ex-

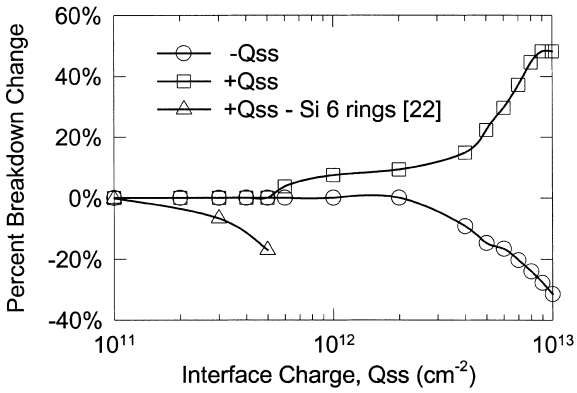

Fig. 6. Comparison between simulated and measured breakdown of diodes with one and two guard rings. For the two ring case, the first ring spacing (S_1) is set at 2 μm and the second ring spacing (S_2) is varied.

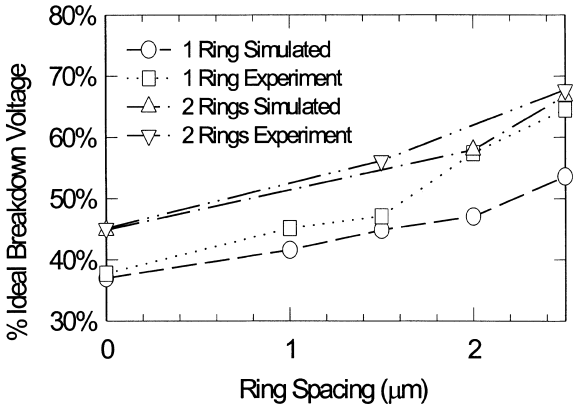

Fig. 7. The correlation between simulated and measured breakdown voltages for diodes with one to four guard rings.

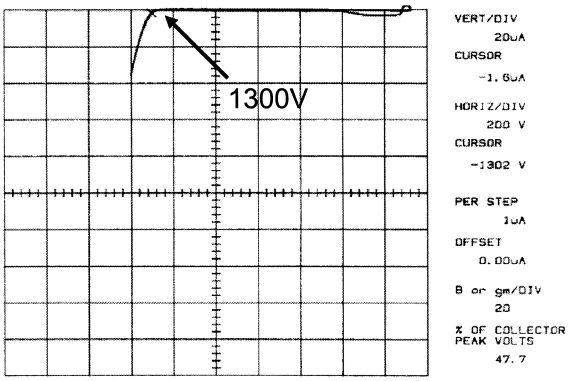

Fig. 8. Output plot of a Tektronix 371 curve tracer showing a breakdown of over 1300 V for a 100 μm implanted diode with four optimized guard rings.

hibited an increase in breakdown voltage from an average of 580 V with no termination, to over 1200 V with four optimized guard rings. The largest measured breakdown voltage, plotted in Fig. 8, was over 1300 V for a 100 μm diameter diode with multiple guard rings. Breakdown was not catastrophic for the diodes tested, demonstrating the termination's effectiveness at limiting the high fields to the bulk material.

5. Summary

We have demonstrated the effective design and implementation of a multiple floating guard ring structure for SiC planar junctions. Breakdown voltages reaching 80% of the ideal parallel plane value were predicted. The high measured breakdown values for these optimized structures is comparable to other reported SiC edge termination techniques, but requires fewer processing steps and is easily transferable to other SiC power devices. Simulated results have also shown that the small inter-ring spacing of SiC guard rings can reduce the effects of unwanted surface charge on the termination design.

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